MOSFET selection for low voltage UPS

Design guidelines

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About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to selecting the correct MOSFET for use in the inverter stage of a UPS operating from a 12 V or 24 V battery. Push-pull and full-bridge topologies are described in square-wave and sine-wave output designs. Paralleling of MOSFETs is also discussed, including thermal considerations, PCB layout optimization and techniques for obtaining best current sharing during steady-state and switching operation.

Intended audience

Design engineers, applications engineers and students.

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1 Introduction

1.1 Uninterruptible power supply types

AC Uninterruptible Power Supply (UPS) systems cover a wide range of power, from single-phase systems rated at less than 1 kVA to three-phase systems rated at over 1000 kVA. Higher-power systems from 5 to 10 kVA upward, designed for large installations and data centers, generally utilize IGBT power devices and modules, which operate from battery banks with voltages in the range of hundreds of volts. Smaller-scale systems for use in small office or home office environments (known as SOHO) often include MOSFET-based inverters that operate from 12 V or 24 V batteries. 24 V systems are sometimes comprised of two series-connected 12 V batteries. Higher battery voltages are required to limit operating currents in higher power rated systems. 42 V and 72 V systems also exist for the same reason; however, since these are somewhat less common, this paper focuses on 12 V and 24 V designs. Different types of rechargeable batteries are used, which may be external or internal to the UPS.

UPS systems can be classified into three main categories (see Figures 1, 2 and 3):

1. *Offline/standby*
   When AC-line voltage is present a relay bypasses the inverter, which remains off. The battery charger operates to maintain full charge. If the AC power fails, the relay switches the UPS output over to the inverter, which starts up after a short interruption of 10 to 20 ms to supply back-up power.

2. *Line interactive*
   Similar to the offline UPS but includes some AC-line conditioning function to regulate the AC output to compensate for low- and high-line input voltage conditions and provide a more stable output voltage. The system is a line conditioner and offline UPS combined.

3. *Online/double-conversion*
   The AC input is converted to DC at the battery charge level and then converted back to AC so that in the event of an AC-line failure the system will switch seamlessly to battery back-up and the output will continue to run without interruption. Such systems provide a stable and clean AC output under all conditions, but there is an inherent efficiency loss with stages of conversion. More sophisticated systems are able to mitigate this by partially bypassing the two conversion stages during AC-line operation, so that only a small amount of power passes through them. If AC input fails the inverter stage is able to take the full load without interruption of the output.

Among SOHO UPS systems (which are the focus of this application note) there are several different types. The most basic units produce an unregulated 50 to 60 Hz square-wave output. These systems are based on LF iron-cored transformers. Sine-wave output inverters are preferred, however, since they offer better power quality and regulated output voltage. These can be further sub-divided into units that also use LF iron-cored transformers and others that use HF ferrite transformers. In both cases the transformer primary is driven by a Pulse Width Modulated (PWM) switching voltage, usually in the 20 to 50 kHz range, with the secondary connected to the output with a capacitor to filter out the HF component, leaving a LF sinusoidal output.

Some UPS systems contain separate battery charger and inverter circuits, whereas others use a single bi-directional converter able to perform both functions. Bi-directional charger-inverter topologies are often used with LF transformers that step down AC voltage in charger mode and step up in inverter mode.

The type of transformer and battery used depends on the specific UPS end use application. For example, a portable unit for outdoor use would contain smaller batteries such as lithium-ion types, and may include a solar charging option, whereas a home or small office-based unit may be connected to bulky external lead-acid batteries. Among these various types of UPS there are several different inverter and charger topologies used.

MOSFET selection criteria will be considered for different inverter and bi-directional charger/inverter architectures.

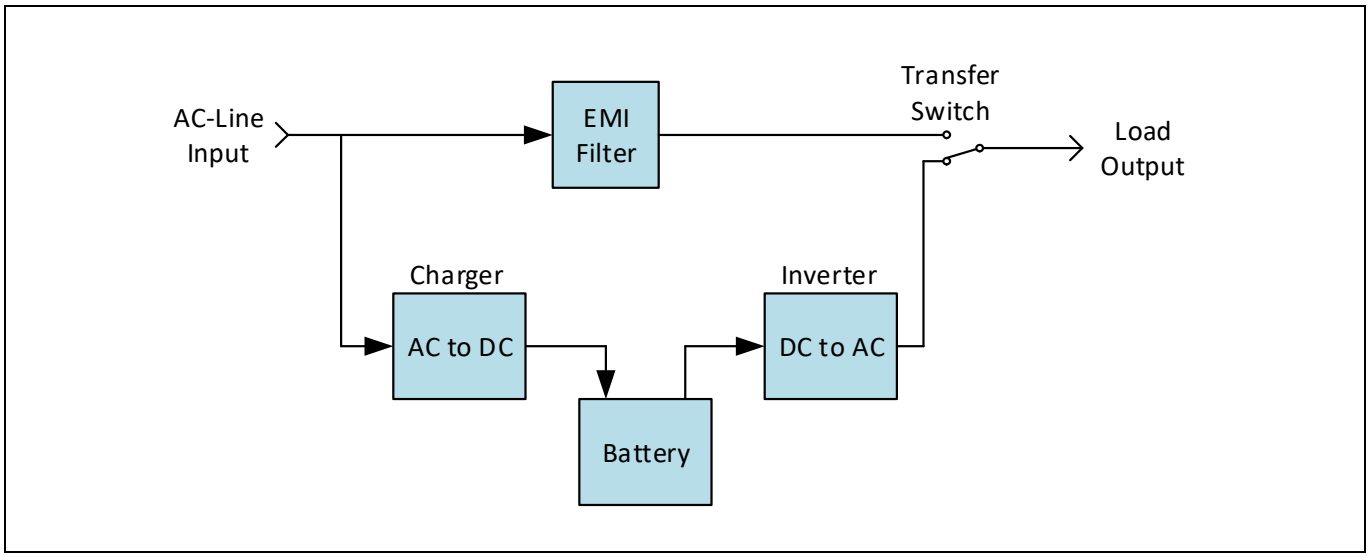

Figure 1 Offline UPS block diagram

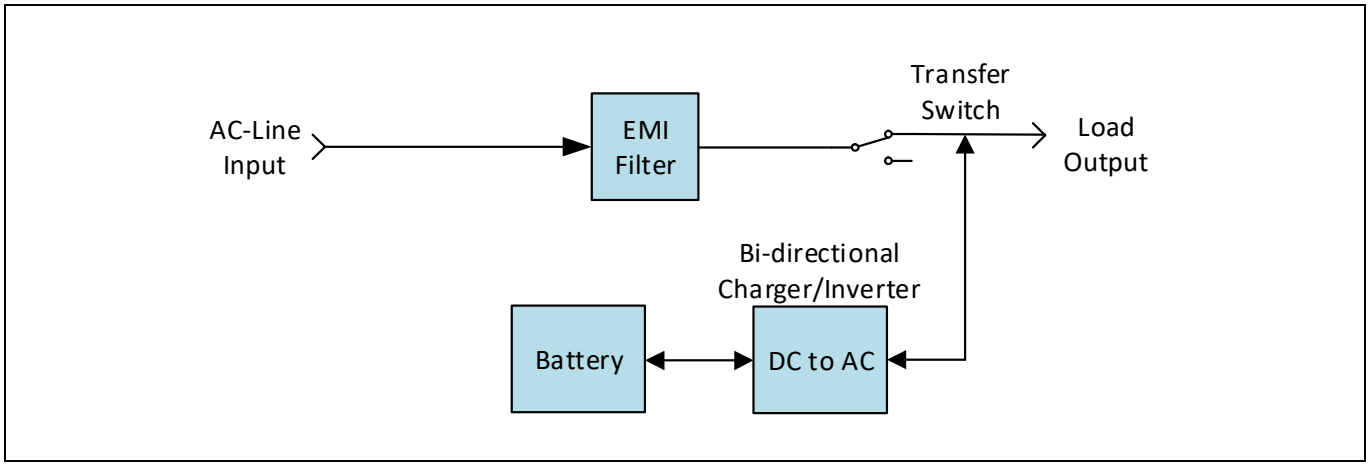

Figure 2 Bi-directional offline UPS block diagram

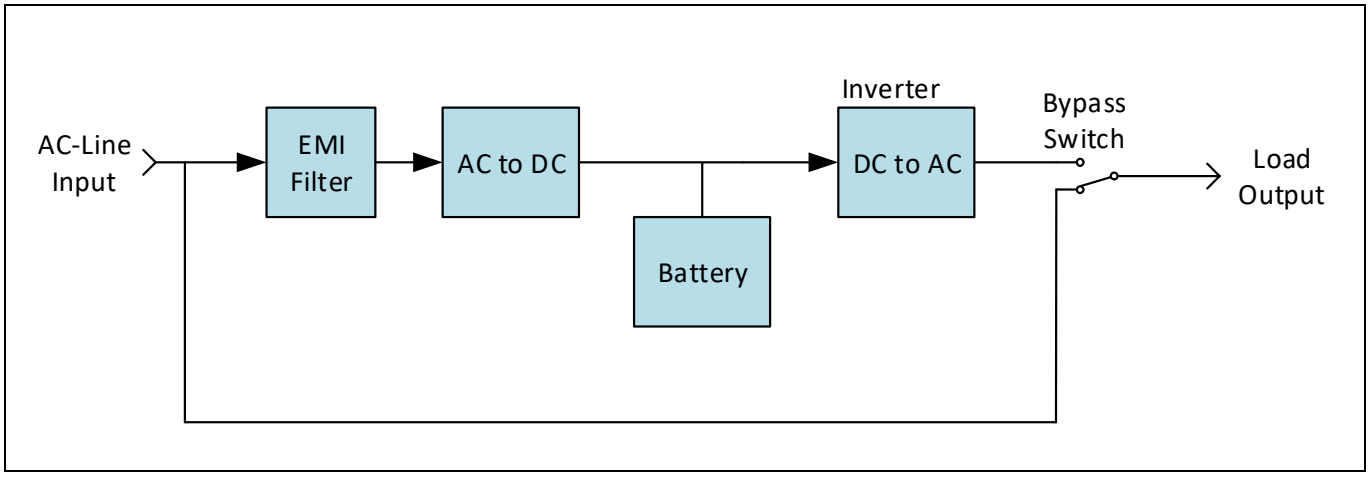

Figure 3 Online UPS block diagram

2 UPS inverter topologies

This paper focuses on the selection of MOSFETs for the inverter or bi-directional inverter/charger of the UPS. Some systems utilize a separate battery charger, which typically consists of a single-switch flyback converter based around a HV superjunction MOSFET. The CoolMOS™ P7 family is recommended for this purpose.

The inverter for low-power (SOHO) UPS systems is usually supplied from a 12 V or 24 V battery voltage, which is connected to the primary winding of a step-up transformer through either a push-pull or full-bridge (or H-bridge) converter. Higher battery voltages are used in higher power rated systems. The first MOSFET selection criterion is the maximum voltage rating BV_{DSS}, which depends on both battery voltage and topology allowing sufficient headroom for transients and surges. Secondly the maximum peak and average current in each MOSFET must be considered based under the maximum load condition and lowest battery voltage. Power MOSFET maximum current handling capability is ordinarily based on package limitation rather than the maximum capability of the die itself. In many cases two or more parallel MOSFETs are used to form each switch in the converter to allow the current and heat dissipation to be shared between devices. Added complications are introduced when MOSFETs are connected in parallel, such as how to accomplish the most equal current sharing possible both in the fully on state and during on and off switching transitions. Mis-matched device parameters result in one device taking a greater share of the current and power losses, potentially operating outside of its Safe Operating Area (SOA) and possibly leading to early failure.

In a square-wave output system the transformer is driven at the line frequency with a duty cycle close to 50 percent. A small dead-time is necessary to prevent shoot-through. In such systems the output voltage is unregulated and proportional to the battery voltage.

Push-pull and full-bridge inverter topologies are widely used in UPS systems, since they utilize the transformer efficiency by operating in two quadrants of the B-H curve to maximize throughput power capability for available volume. In both cases the instantaneous output voltage is given by:

$$V_{OUT} = (+/-)\frac{N_S}{N_P} \cdot V_{IN} \quad [1]$$

Where V_{IN} is equal to the DC bus voltage and N_S/N_P is the transformer turns ratio (voltage drops on the switches are negligible). In the push-pull transformer the primary is N_P, which refers to the turns between the center-tapped primary and one end of the winding. In the full-bridge it refers to the total primary turns. In square-wave systems the transformer secondary voltage is the inverter output, which can be positive or negative.

In sine-wave systems transformer is driven by a HF PWM switching voltage above the audible range, and the output is filtered so that:

$$V_{OUT}(t) = \frac{N_S}{N_P} \cdot D(t) \cdot V_{IN} \quad [2]$$

A time-varying modulated duty-cycle function D(t) is used to adjust the integrated output voltage $V_{OUT}(t)$. The high leakage inductance inherent in LF transformers is combined with an output capacitor to create a low-pass filter, which removes the HF switching component.

A microcontroller generates the sine-wave modulated gate-drive pulses. The switching frequency used is a trade-off of switching losses, transformer core losses and clock speed against size and volume of magnetic components and capacitors. Note that in equation [2] D refers to the PWM command duty cycle, which can vary between zero and one. This is divided into two alternating gate-drive pulses such that each switch is operated every other pulse and therefore the actual gate drive maximum duty cycle $D_{G(MAX)}$ is 0.5. The duty-cycle granularity is limited by microcontroller clock speed, and therefore a lower PWM frequency just above the audio range at around 20 kHz provides the best resolution. The modulation index (m) determines the amount by which the duty cycle is modulated and is controlled to provide regulation of the RMS AC output voltage.

2.1 Low frequency transformer based UPS

2.1.1 Push-pull topology

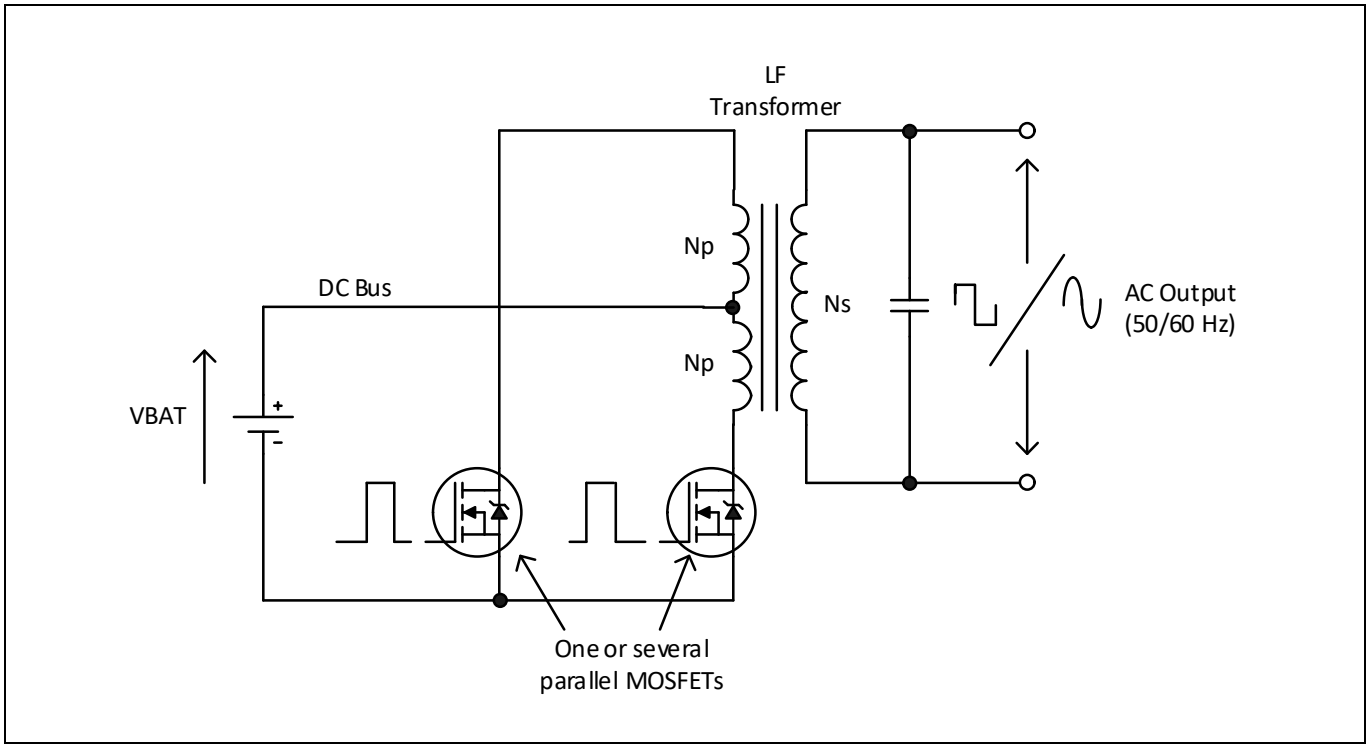

Figure 4 Push-pull basic schematic

The push-pull topology requires only two switches, since the transformer primary center-tap is connected to the DC bus. However this has the disadvantage that during their respective off periods, twice the battery voltage appears at the drain of each MOSFET. It is necessary therefore to select devices with BV_{DSS} ratings of at least twice the maximum battery voltage plus enough headroom to allow for transients and surges.

Additionally, in a bi-directional charger-inverter a high AC-line condition must also be taken into account in determining the required BV_{DSS}. In some countries the AC mains voltage is known to vary over a wide range; in certain cases a nominal voltage of 220 V AC can rise to as high as 350 V AC. As the transformer is acting as a step down during charger mode, the MOSFETs will be exposed to the highest drain voltage during a high-line condition.

For a square-wave UPS the primary current is an approximate square wave with a small magnetizing current ramp added. This is shown in the blue waveform in Figure 5, which shows the current measured with a probe clamped around both end leads of the transformer primary connected to the drains of each MOSFET. The transformer is designed to keep its size and volume as small as possible and it is therefore driven farther up the B-H curve toward saturation, accounting for the rise in magnetizing current at the end of each switching cycle.

The red and green waveforms are the drain voltages, reaching double the voltage of the nominally 12 V battery. The yellow waveform is the gate drive to one of the MOSFETs. The primary current is approximately 70 A in this example, corresponding to a load of approximately 840 W. The switching frequency is 50 Hz.

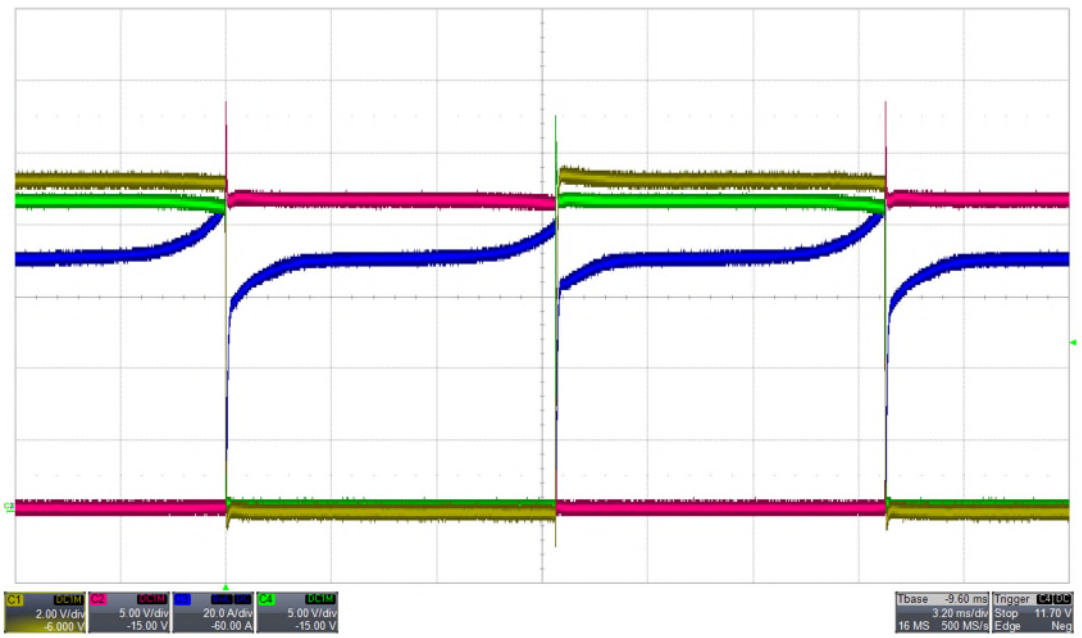

Figure 5 Square-wave push-pull UPS voltage and current waveforms

The push-pull topology driving a LF transformer is not fully bi-directional, because although in charger mode rectification is possible through the MOSFET body diodes, there is no way the MOSFETs can regulate the charge current to the battery. It is necessary to add a regulating element such as a triac at the secondary (HV) side. This however produces high peak current and low power factor.

A further complication exists due to the very different crest factors[1] of the square-wave voltage generated in back-up/inverter mode, and the sine-wave voltage from the AC-line in charging mode. It becomes necessary to select a different number of turns at the transformer secondary during the charging operation, which requires an additional relay.

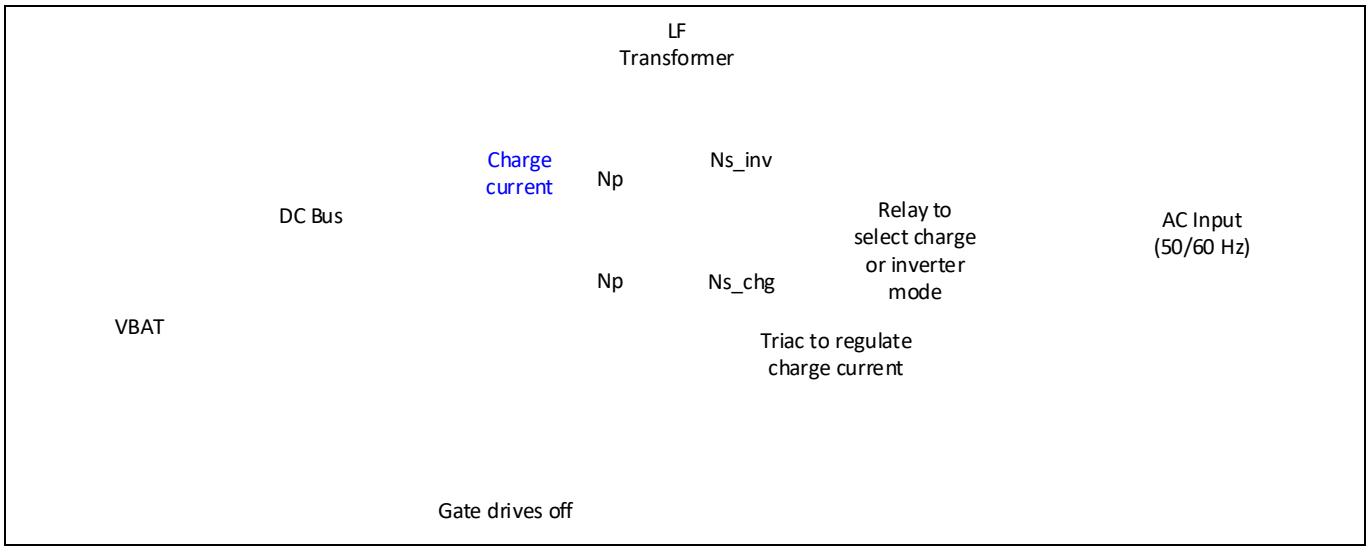

Figure 6 Push-pull UPS charging scheme

[1] Crest factor is defined as the ratio of the peak to the RMS value of an AC waveform.

The above figure shows that the transformer secondary has two taps; these select different turns ratios for inverter mode and for charging mode. The system switches between these via the relay, which is controlled through and opto-isolator from the primary controller. The average charge current is regulated by adjusting the pulse width of the triac gate-drive waveform, shown in red. This is also driven through an opto-isolator from the primary-side controller IC.

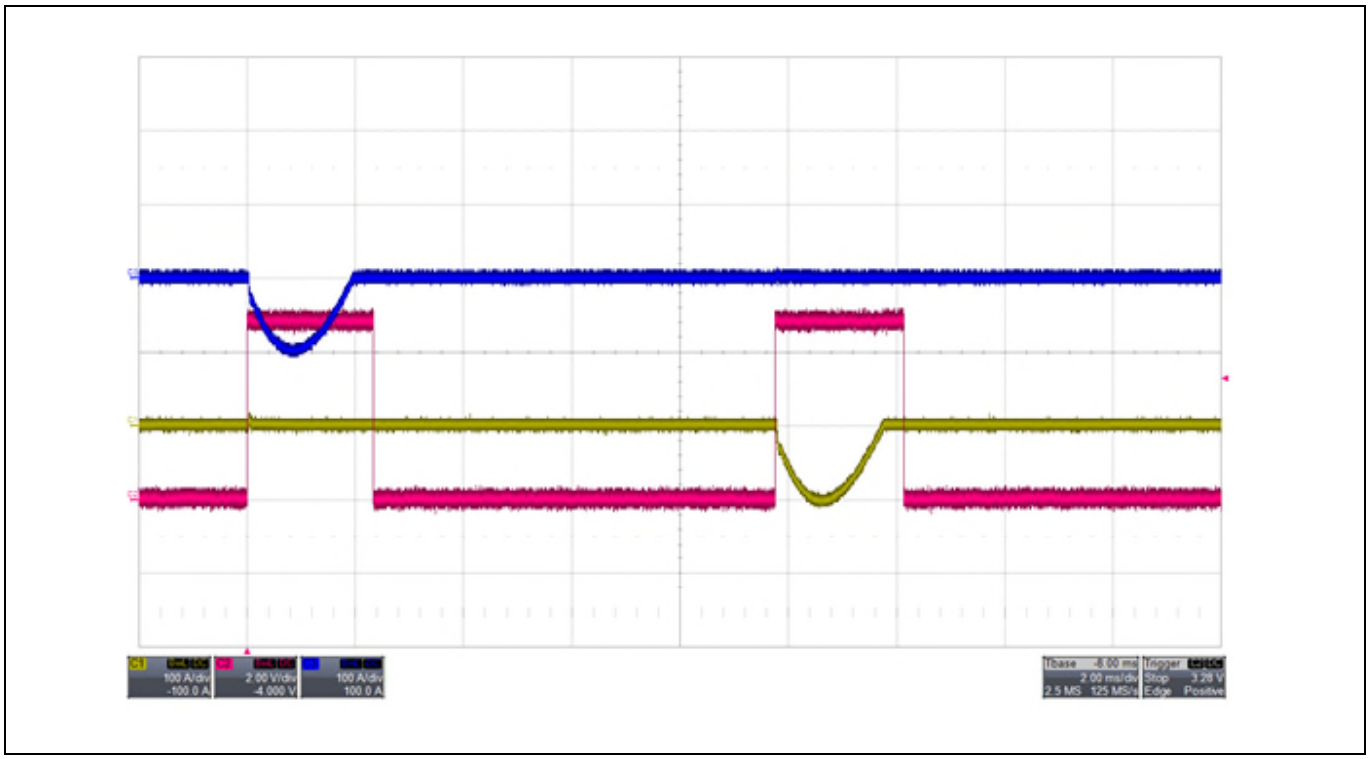

Figure 7 Push-pull UPS charge current waveform

The above waveforms show the currents measured at each of the transformer primary connections (blue and yellow traces). These currents are equal to that passing through each branch of the push-pull circuit, including the parallel body diodes of each set of MOSFETs during charging. The scale is 100 A/div at 2 ms/div, indicating a peak current of 100 A.

Push-pull inverters are gradually being superseded by more efficient full-bridge designs, which can provide the same output power with a smaller transformer.

2.1.2 Full-bridge topology

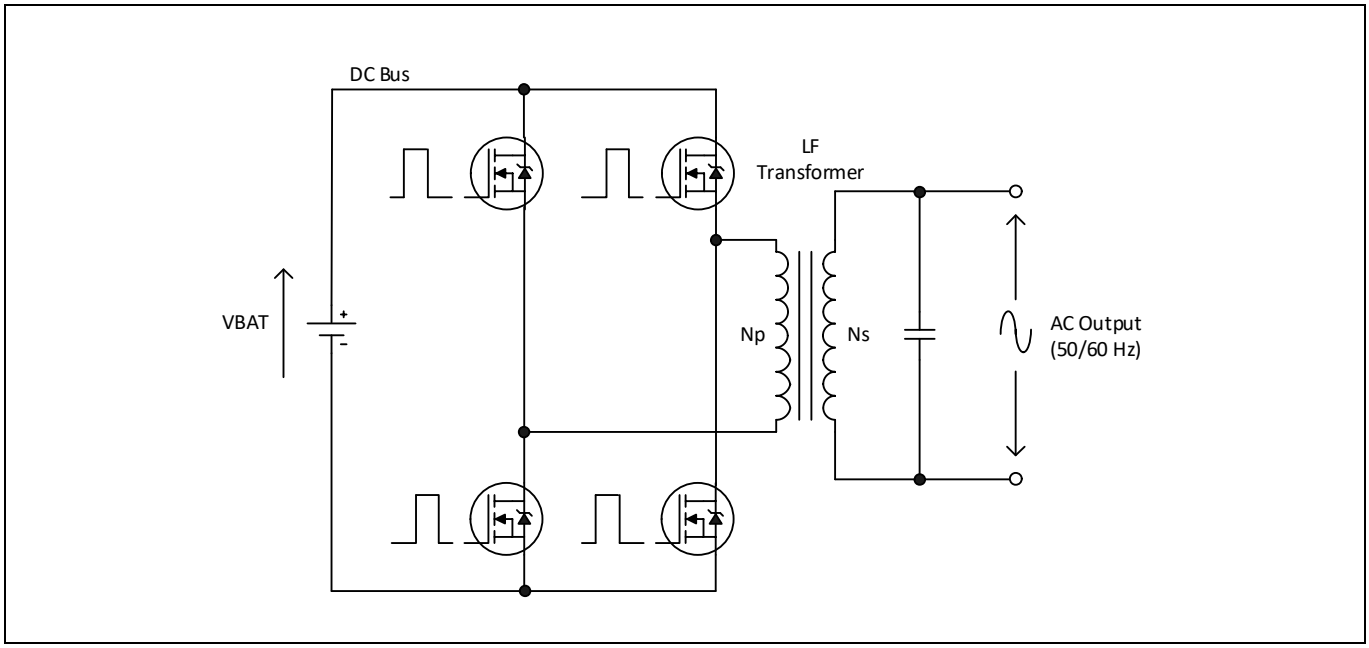

Figure 8 Full-bridge basic schematic

The full-bridge inverter consists of four switches, which typically consist of a bank of parallel MOSFETs to carry the high current. The maximum drain voltage remains at one body diode drop above the battery voltage apart from a small switch-off transient, therefore the BV_{DSS} rating may be selected based on the highest battery voltage with some appropriate headroom allowed in case of abnormal conditions. One advantage over the push-pull topology is that the transformer primary winding is driven in both polarities without the need for a center tap, which allows volume reduction. However, the drawback is that the full-bridge requires two floating high-side gate drivers.

2.1.2.1 Back-up mode operation

During inverter operation each half-bridge side of the full-bridge operates as a synchronous buck converter in Continuous Conduction Mode (CCM) connected to one side of the transformer primary. The other side is typically connected to the battery positive via the opposite high-side MOSFET. A high-side/low-side driver IC is used to supply the gate drives to each of the half-bridges. The reason for making the low-side MOSFETs the buck main switching elements is because these are hard-switched, while the upper MOSFETs operating synchronously are soft-switched. A dead-time is included to prevent any high current shoot-through. Floating high-side gate-drive outputs from half-bridge driver ICs are more sensitive to potential latch-up, dv/dt or negative voltage transitions when driving hard-switched MOSFETs, which is not normally an issue with soft-switching. Since the low-side gate driver is not floating it is much better suited to driving hard-switched MOSFETs.

The HF switching side of the full-bridge alternates depending on the direction of the transformer primary current to provide the positive and negative output voltage half-cycles. Whichever side of the full-bridge is operating in buck mode controls the output voltage by PWM of the low-side MOSFET duty cycle. This is modulated to produce a sinusoidal output voltage at the line frequency.

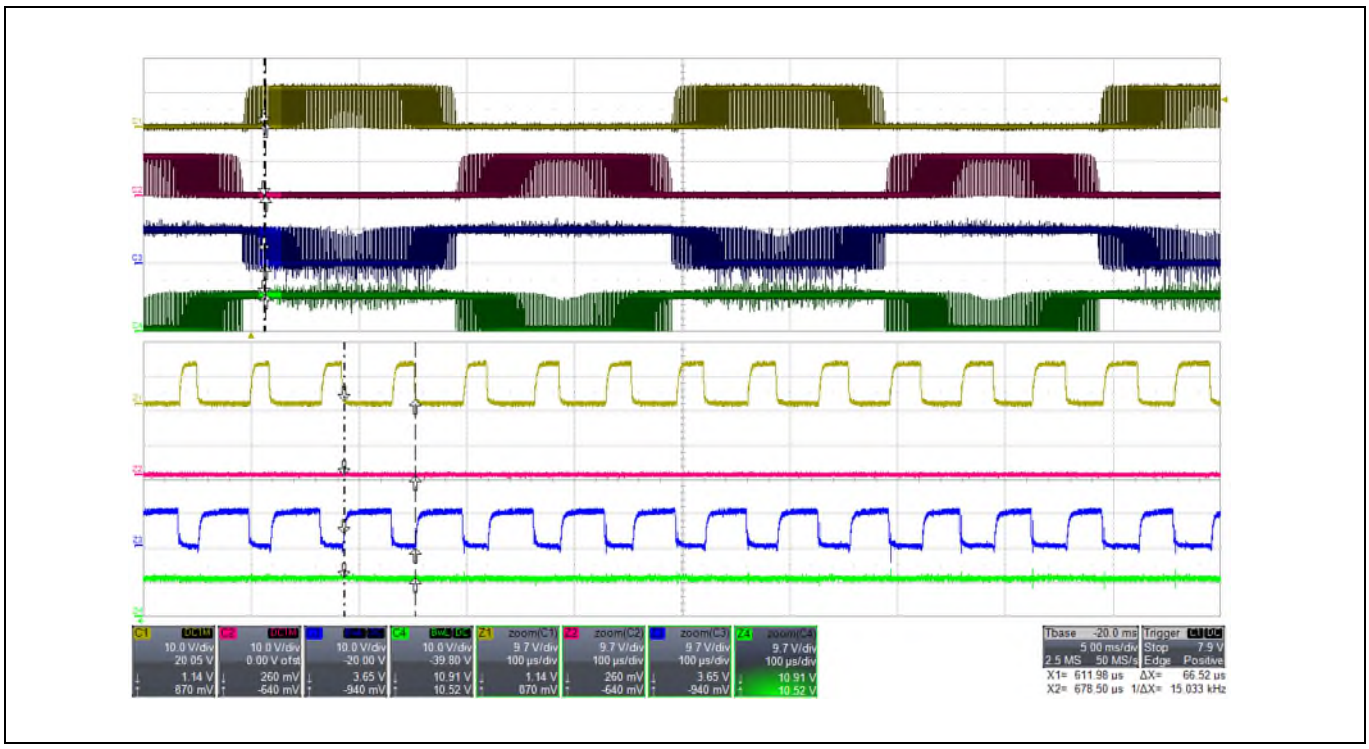

Figure 9 Inverter mode gate-drive waveforms

The gate-drive waveforms for each full-bridge MOSFET during inverter operation are shown above. The blue trace is one high-side, with the yellow trace its corresponding low-side. The green trace is the opposite high-side and the red is the low-side.

2.1.2.2 Charging mode operation

An added advantage of the topology is that it enables a fully bi-directional inverter/charger to be realized. In battery charging mode it is able to operate as a form of bridgeless PFC boost converter to provide regulated battery charge current, while drawing a roughly sinusoidal phase current from the AC supply. The transformer primary leakage inductance acts as the Boost inductor supplied with voltage stepped down from the AC-line.

Should the battery voltage be lower than the secondary peak voltage (see Figure 10) minus two body diode drops, then uncontrolled current would flow into the battery. To avoid this a resettable fuse is often added in the UPS AC output. This offers protection against overload, abnormally low battery voltage or short circuit of the battery connections.

This charging scheme may be used in sine-wave or square-wave output full-bridge UPS systems. However, in the square-wave system a secondary winding tap change via a relay is necessary to compensate for different peak-to-RMS voltage ratios between the sine-wave charging voltage supplied by the AC-line and the square-wave output voltage produced by the inverter. This is necessary to maintain the rectified AC-line voltage low enough to allow bridgeless boost charging.

In bridgeless boost charging mode the two upper switches MH1 and MH2 are typically always off, and the lower switches ML1 and ML2 are both driven on and off together by PWM pulses at the switching frequency. Depending on the AC-line polarity boost operation will occur in one or other of the branches of the bridge.

Operation can be understood by considering the transformer primary as a voltage source with a series inductor to represent the lumped primary and secondary leakage inductances.

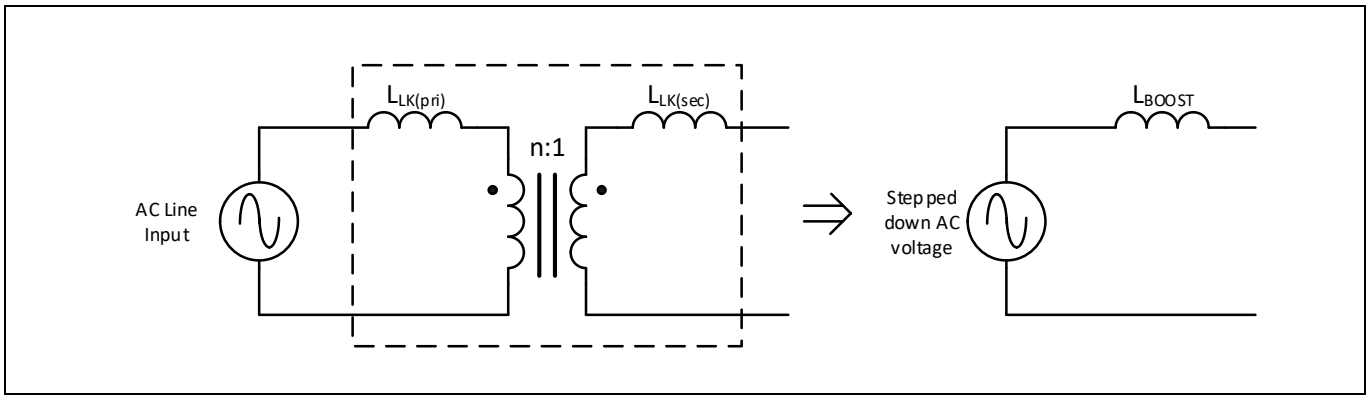

Figure 10 Transformer equivalent circuit in charging operation

When both lower switches are on current rises in the inductor and energy builds up in the magnetic flux. When they are both switched off, the inductor current passes through the body diodes in one diagonal pair of MOSFETs depending on its direction according to the AC-line half cycle polarity. The MOSFET body diodes thus form a bridge providing a DC charge current to the battery.

The feedback loop regulating the battery charge current is necessarily slow so that changes in duty cycle happen gradually over several AC-line cycles in the same way that they do in PFC converters. This allows line current to form a more sinusoidal shape to more closely follow the AC line voltage and thus improve the power factor, typically to above 0.8.

Power Factor Correction (PFC) can therefore be implemented during charging without the need for any additional components, simply by driving the MOSFETs differently.

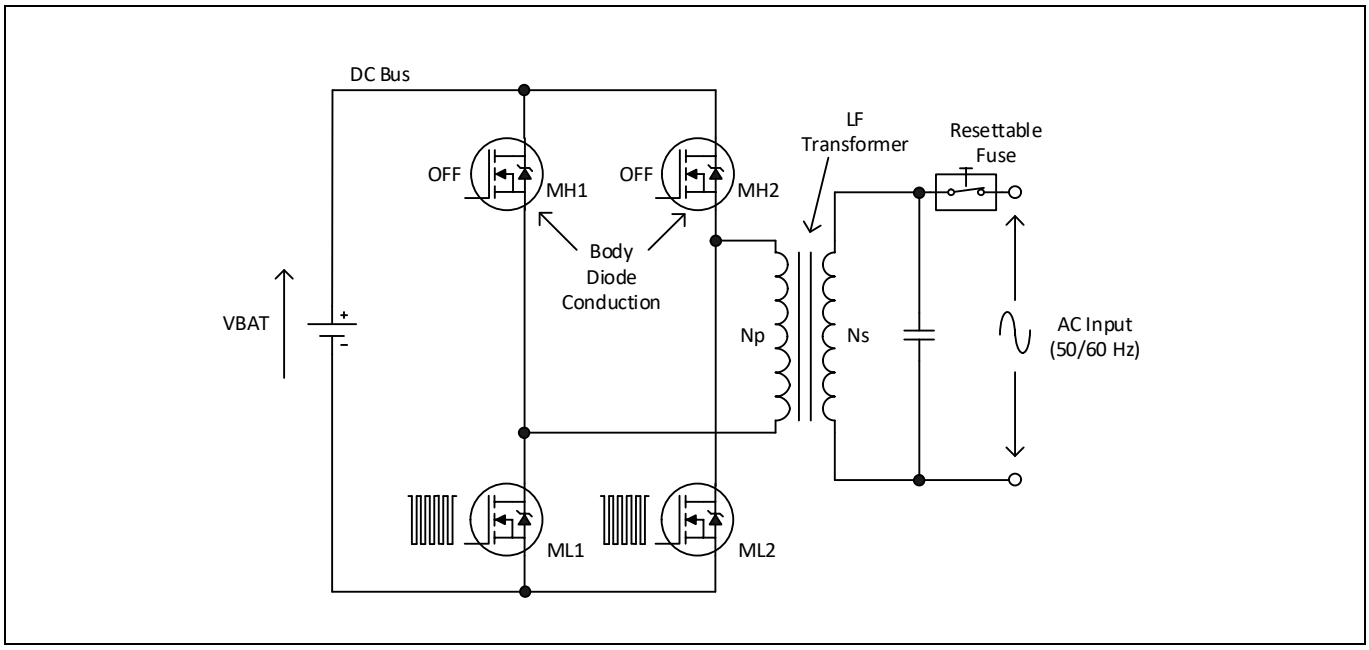

Figure 11 Bridgeless boost PFC charging

2.2 High frequency transformer-based UPS

High frequency transformers are typically used in multi-stage UPS topologies, which can be either offline (standby) or online (double conversion) types. These architectures are used in portable units, or where size and weight are important. Such systems are not generally bi-directional, utilizing a separate converter for the battery charger. The inverter consists of an isolated DC-DC step-up stage to convert the battery voltage to a HV DC bus voltage, followed by an inverter stage that produces a sinusoidal output voltage at 50 or 60 Hz. The DC-AC stage is non-isolated and non-regulated.

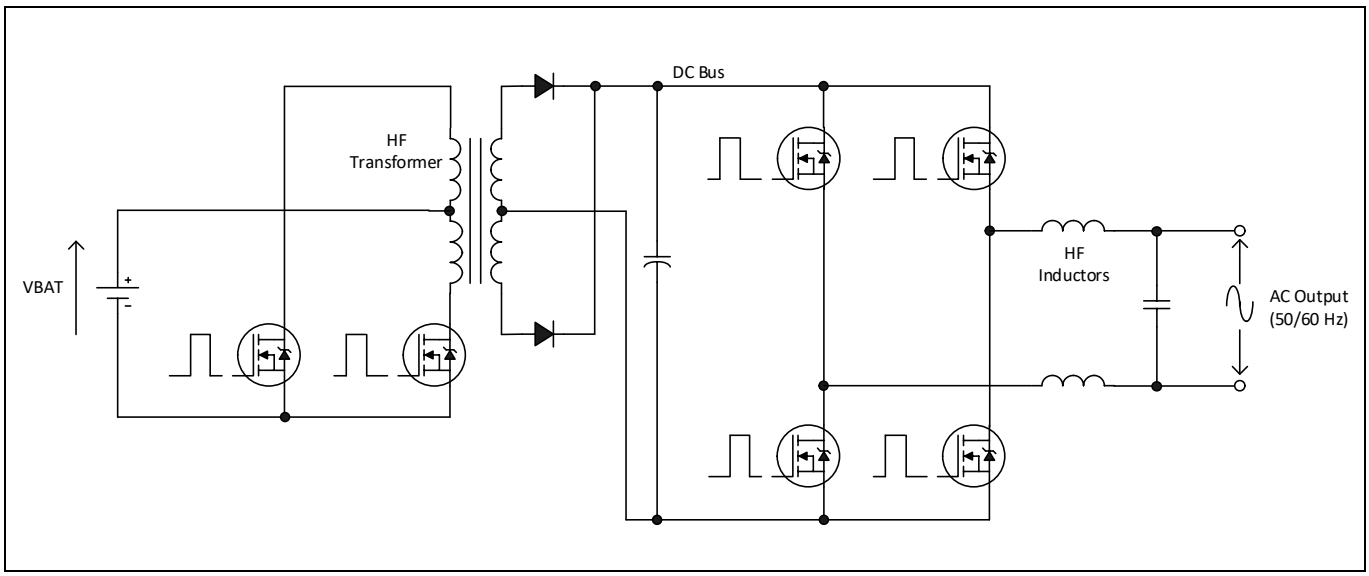

Figure 12 HF transformer based UPS inverter block diagram

In the typical example shown in Figure 12, the DC-DC stage uses a push-pull topology with a split primary and secondary HF transformer winding to produce the DC bus voltage. This stage may be a conventional hard-switching push-pull converter with optional PWM regulation of the output bus voltage, or alternatively it could be a Zero Voltage Switching (ZVS) push-pull converter, which is operated at a fixed duty cycle close to 50 percent in open loop. In this case the DC bus voltage would vary according to battery terminal voltage and load, and all regulation would be done in the output stage.

The DC-AC stage is a full-bridge followed by an LC filter that produces the sinusoidal output from modulated PWM switched voltage waveforms typically at around 20 kHz. All of the magnetic components are therefore wound on ferrite cores. This is not a bi-directional topology; however, the DC bus capacitor is charged through the full-bridge MOSFET body diodes when AC mains voltage is present and the MOSFETs are all off. A separate converter may be supplied from this voltage to provide regulated battery charging. A flyback converter is often used for this purpose due to simplicity and low component count.

It is important to consider the short-circuit output condition when selecting suitable MOSFETs for the inverter stage. Discharge of the bus capacitor creates a very high pulse current, which is not greatly limited by the HF output filter inductors. The MOSFET pulse current rating must be sufficient to withstand this fault condition.

‘

3 MOSFET selection criteria

3.1 Selecting BV_{DSS}

The combination of MOSFETs to be used in a LF transformer-based UPS depends on the battery voltage, the inverter topology and, in the case of systems based on LF transformers, the maximum high-line voltage to which the system may be connected as well as the total power. The first parameter to be considered is the maximum voltage rating BV_{DSS}, which is determined initially according to the maximum battery voltage and the topology. For a lead-acid battery the terminal voltage may be up to 15 V. In a push pull topology BV_{DSS} must allow for $2 \times V_{BAT(MAX)}$ and for full-bridge $V_{BAT(MAX)}$, which will appear at the drain. Since these are usually hard-switching topologies transient voltages will be present resulting from body diode recovery, therefore to avoid placing unnecessary stress on the devices, it is advisable to allow 100 percent extra voltage margin to avoid avalanching due to these spikes. For example, a full-bridge system operating with a 24 V battery should use 55 or 60 V rated MOSFETs. This would also apply for a 12 V push-pull system, but 30 V MOSFETs should be sufficient for a 12 V full-bridge system. It should be noted that the full-bridge clamps the leakage inductance energy to the battery voltage through the body diodes, and therefore transients are less than in the push-pull case. In HF transformer-based UPS topologies these criteria also apply for the DC-DC stage. In the back end inverter stage HV CoolMOS™ devices suitable for hard-switching operation are recommended. Here again a good safety margin is needed to avoid the avalanche condition, particularly under short-circuit where abnormally high voltage spikes are produced.

Table 1 Recommended BV_{DSS} for battery voltage and UPS architecture

Battery voltage (nominal)	UPS architecture	BV_{DSS}
12	Push-pull (low frequency transformer)	55 to 60
	Full-bridge (low frequency transformer)	30 to 40
24	Push-pull (low frequency transformer)	75 to 100
	Full-bridge (low frequency transformer)	40 to 60
48	Push-pull (low frequency transformer)	150
	Full-bridge (low frequency transformer)	100
72	Push-pull (low frequency transformer)	200
	Full-bridge (low frequency transformer)	100 to 150

3.2 Selecting $I_{D(max)}$

Having selected the required BV_{DSS} the next parameter to consider is the maximum continuous current rating $I_{D(MAX)}$. Where the MOSFET datasheet includes maximum silicon limited ratings as well as package or wire bond limited ratings, the lowest value should be used. For temperature de-rating a graph of $I_{D(MAX)}$ against case temperature should be provided, which may be used to determine the maximum current rating at 100 degrees C.

In both push-pull and full-bridge converters during inverter operation the average current in each power switch consisting of one or more parallel MOSFETs will be half the current being supplied from the battery. Therefore the highest current would be at the maximum load rated for the UPS and the lowest battery voltage also factoring in the converter efficiency, which may be estimated at 85 percent. Lead acid batteries should not be operated below a certain minimum voltage level since this causes damage due to sulfation.[1] For a nominally 12 V battery severe damage will occur if it is discharged below 10.5 V. For this reason UPS systems are designed to cut out when the battery voltage drops below a minimum threshold, which may be considered the worst case for calculating the maximum current. For example, a suitable cut-off voltage $V_{BAT(MIN)}$ may be set at 11.6 V, therefore a 1000 W UPS would theoretically draw a maximum current of $1000/(0.85 \times 11.6) = 101.4$ A. The average current passing through each switch would then be 50.7 A.

Having determined the worst-case average current the peak current should then be considered, which will typically be twice the average current assuming that the system is operating close to 50 percent duty cycle at full load and minimum battery voltage. In systems based on high frequency transformers the magnetizing current should also be taken into consideration. It is reasonable to allow an extra 50 percent of safety margin for the peak current.

Having determined the worst-case current for inverter operation it is now necessary for bi-directional charger/inverter topologies to establish what the maximum current during charging will be. Both the average and peak currents vary considerably in different topologies. Obviously this does not apply where separate converters are used for charging. When the worst case average and peak operating currents have been established, the power dissipation of the device and die temperature rise needs to be looked at. The power dissipation includes conduction losses in the channel and body diode during different modes of operation as well as switching losses, which have yet to be discussed.

[1] Sulfation is a chemical reaction that causes coating of both positive and negative battery plates with lead sulfate during a discharge cycle. However, excessive build-up causes permanent damage that cannot be reversed by recharging.

3.3 Switching losses in UPS

As discussed, UPS topologies are generally hard-switching; therefore switching losses must be considered except in special cases such as the ZVS push-pull. Switching losses should not be significant in square-wave UPS systems since the switching frequency is low at 50 or 60 Hz.

In sine-wave systems, however, the switching frequency is typically around 20 kHz operating in continuous conduction mode (CCM) thereby producing switching losses that add a significant contribution to overall device losses and die temperature rise. Body diode reverse recovery also adds to this.

Hard-switching occurs when there is an overlap between voltage and current when switching the MOSFET on and off. The energy loss caused can be minimized by increasing the di/dt and dv/dt, however this leads to more EMI and larger transients.

3.3.1 Push-pull (non-ZVS) converter switching losses

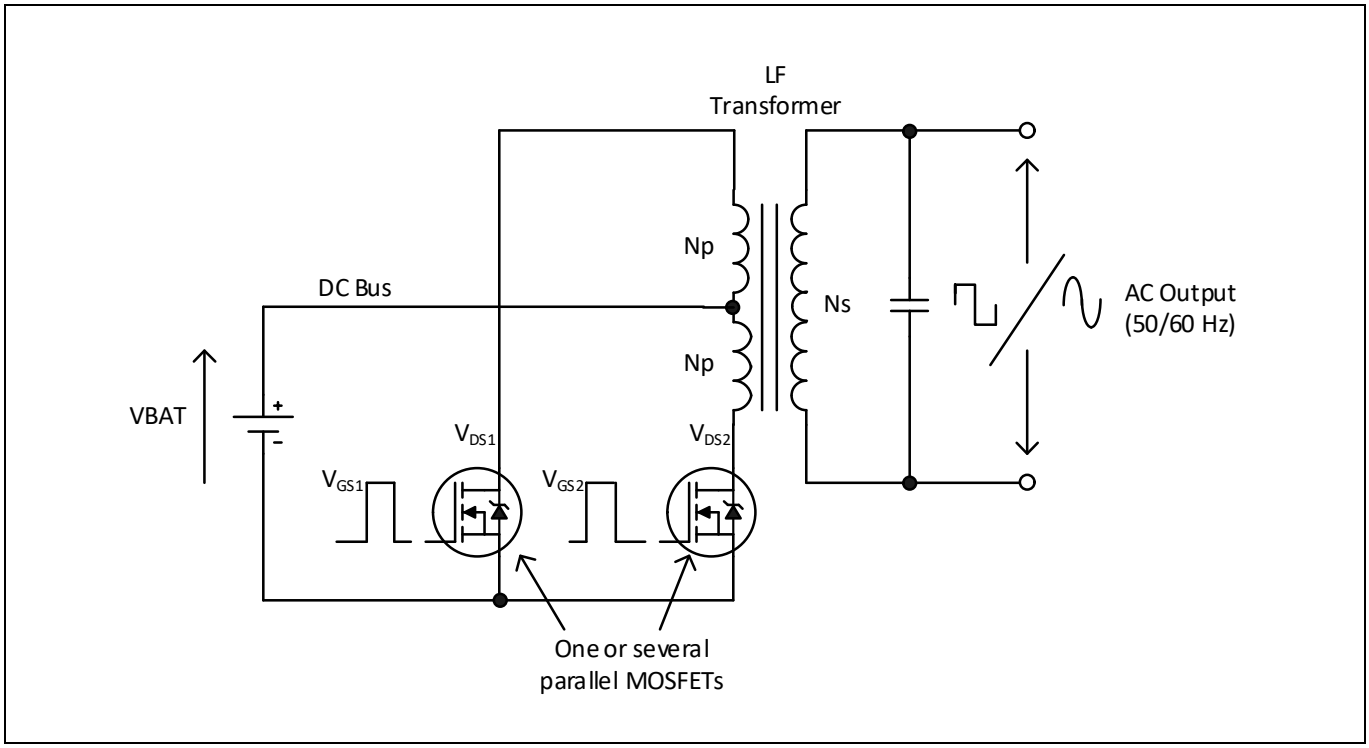

Figure 13 Push-pull inverter switching elements

The gate drive and drain voltage waveforms for each of the banks of parallel MOSFETs from a 1250 W rated square-wave UPS are shown below, with a dead-time of ~500 µs. At switch-off of V_{GS2} the drain voltage V_{DS2} displays the transformer leakage inductance spike typically seen in push-pull converters, which exceeds twice the battery voltage. Unlike in the full-bridge converter the leakage energy is not clamped to the DC bus by the body diodes, further justifying the need for plenty of BV_{DSS} headroom. The gate-drive voltage turn-off plateau is seen as the drain voltage rises. The drain current remains high during this hard-switching transition where the losses are exacerbated by the high drain voltage caused by the leakage energy. As this energy is dissipated the drain voltage falls to the battery voltage for the remainder of the dead-time.

At switch-on the current is zero (ZCS) assuming the UPS is not connected to an inductive load, which would not typically be the case. At switch-on the drain voltage rises from V_{BAT} to 2 × V_{BAT} with negligible losses due to the ZCS operation. While this is true for square-wave UPS systems it would not be the case for sine-wave UPS or the DC-DC stage of a high frequency transformer-based system, because in such systems the output current is effectively continuous during both switching transitions.

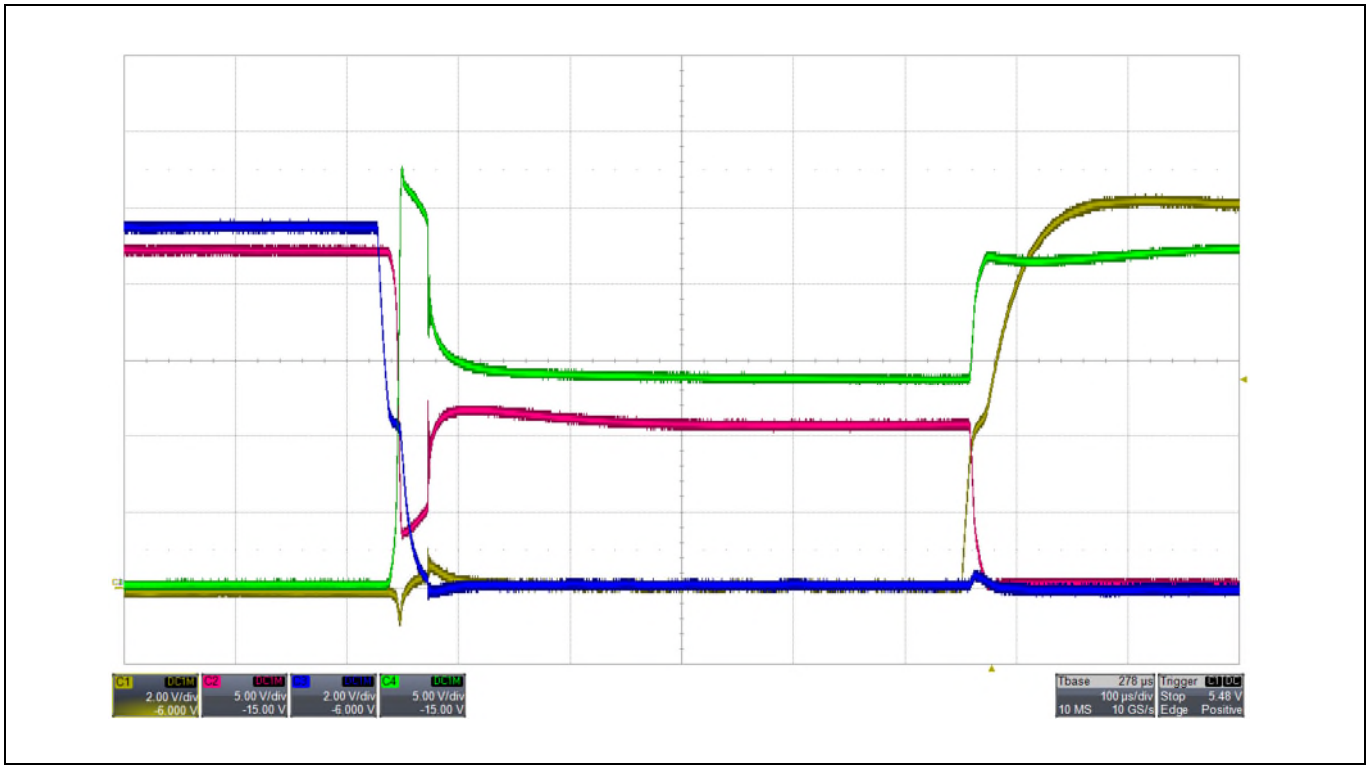

Figure 14 Push-pull inverter switching waveforms
CH1 (yellow): VGS1, CH2 (red): VDS1, CH3 (blue): VGS2, CH4 (green): VGS2

3.3.2 Full-bridge converter switching losses

As in the push-pull converter the full-bridge converter always exhibits a hard switch-off transition. A ZCS switch-on occurs in the case of square-wave inverters but not in sine-wave inverters. A major advantage with the full-bridge is that in this topology the drain voltage is clamped to the battery voltage so that transformer leakage inductance does not result in high drain voltage transients during the hard-switching transitions. Switching losses in the full-bridge can therefore be lower than in the push-pull, provided the gate drive is optimized to minimize the effects of body diode recovery. However in a full-bridge switching losses and conduction losses are produced in four switches instead of two. In spite of this the overall switching losses should still be lower for this topology.

The waveforms shown below show the switch-off drain voltage (VDSL1) transient in a full-bridge square-wave inverter. It is seen that this transient reaches 21 V peak and drops very rapidly down to the battery voltage. The duration of this transient is ~150 ns, which results from the forward recovery time of the body diodes.

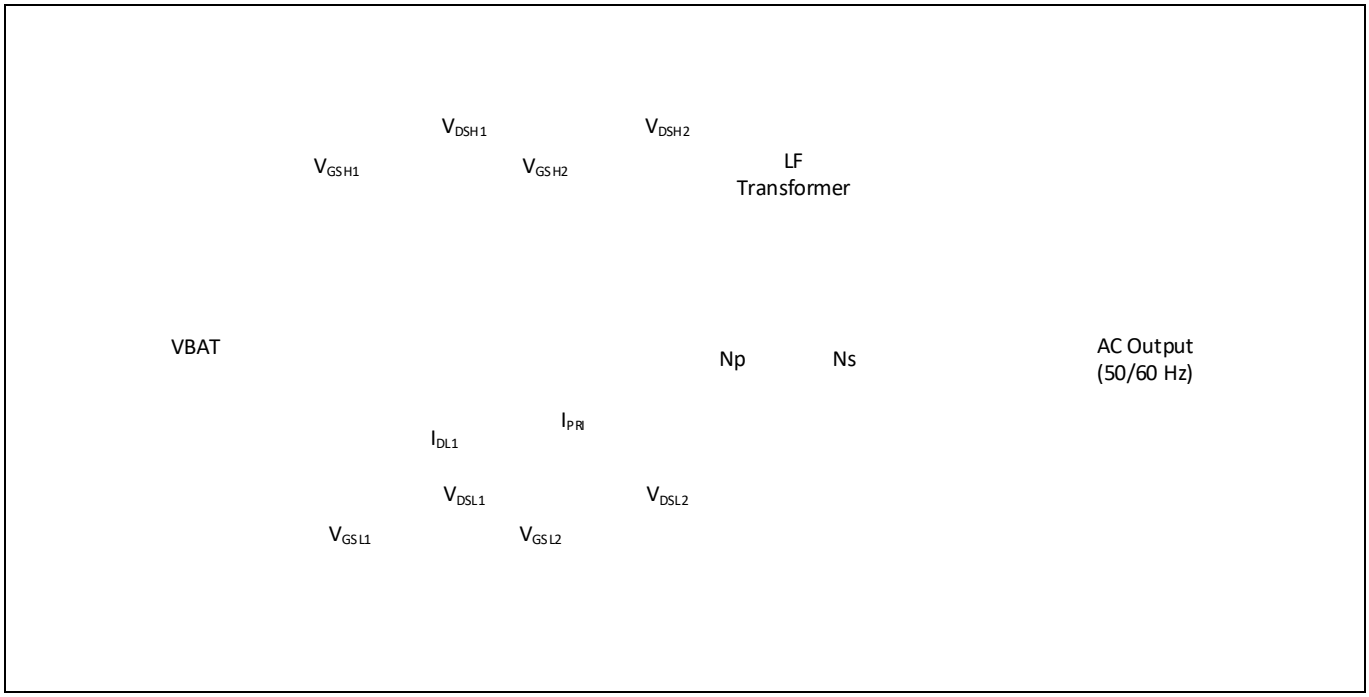

Figure 15 Full-bridge inverter switching elements

In both square and sine-wave implementations ML1 and MH2 are on at the same time, and ML2 and MH1 are on at the same time, with sufficient dead-time included to prevent any cross-conduction.

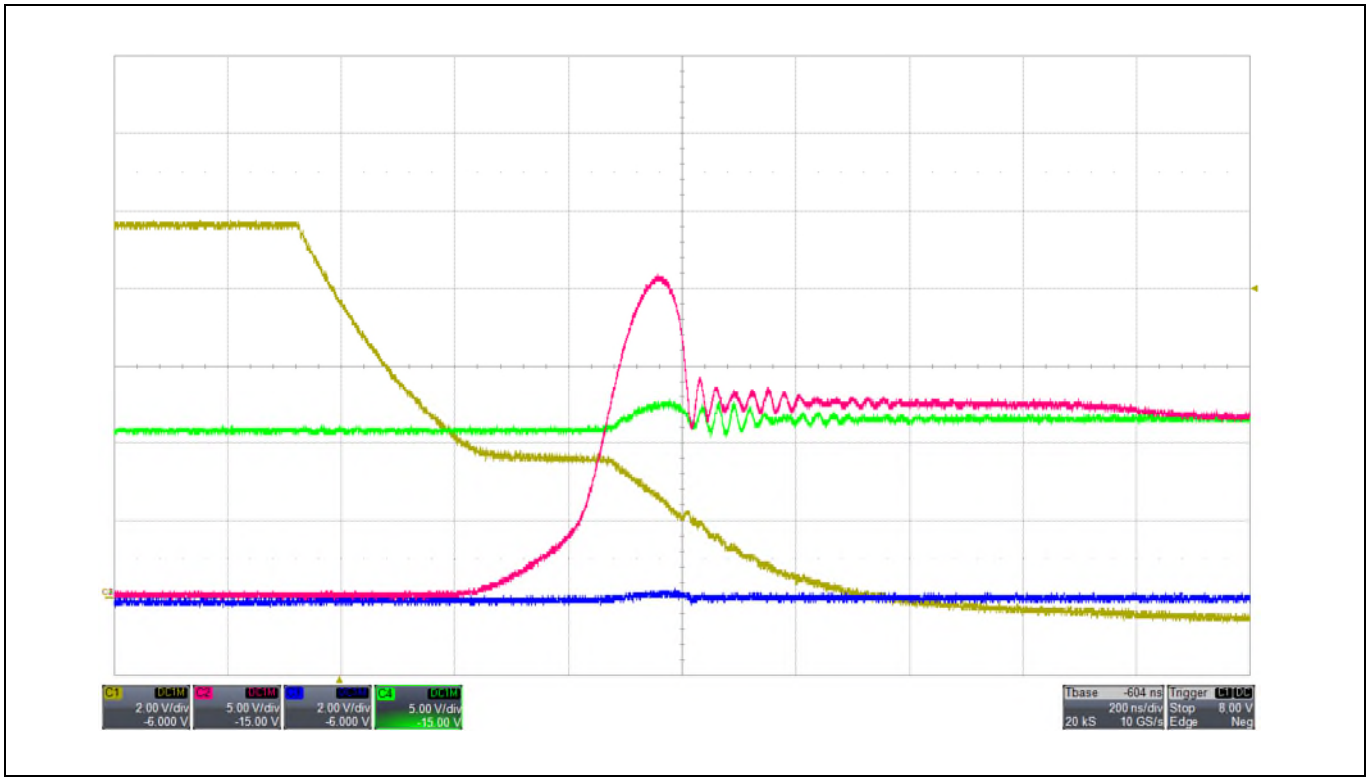

Figure 16 Full-bridge square-wave inverter switching waveforms
CH1 (yellow): VGSL1, CH2 (red): VDSL1, CH3 (blue): VGSL2, CH4 (green): VBAT

The following figures show the hard-switching transitions that occur in the sine-wave full-bridge inverter.

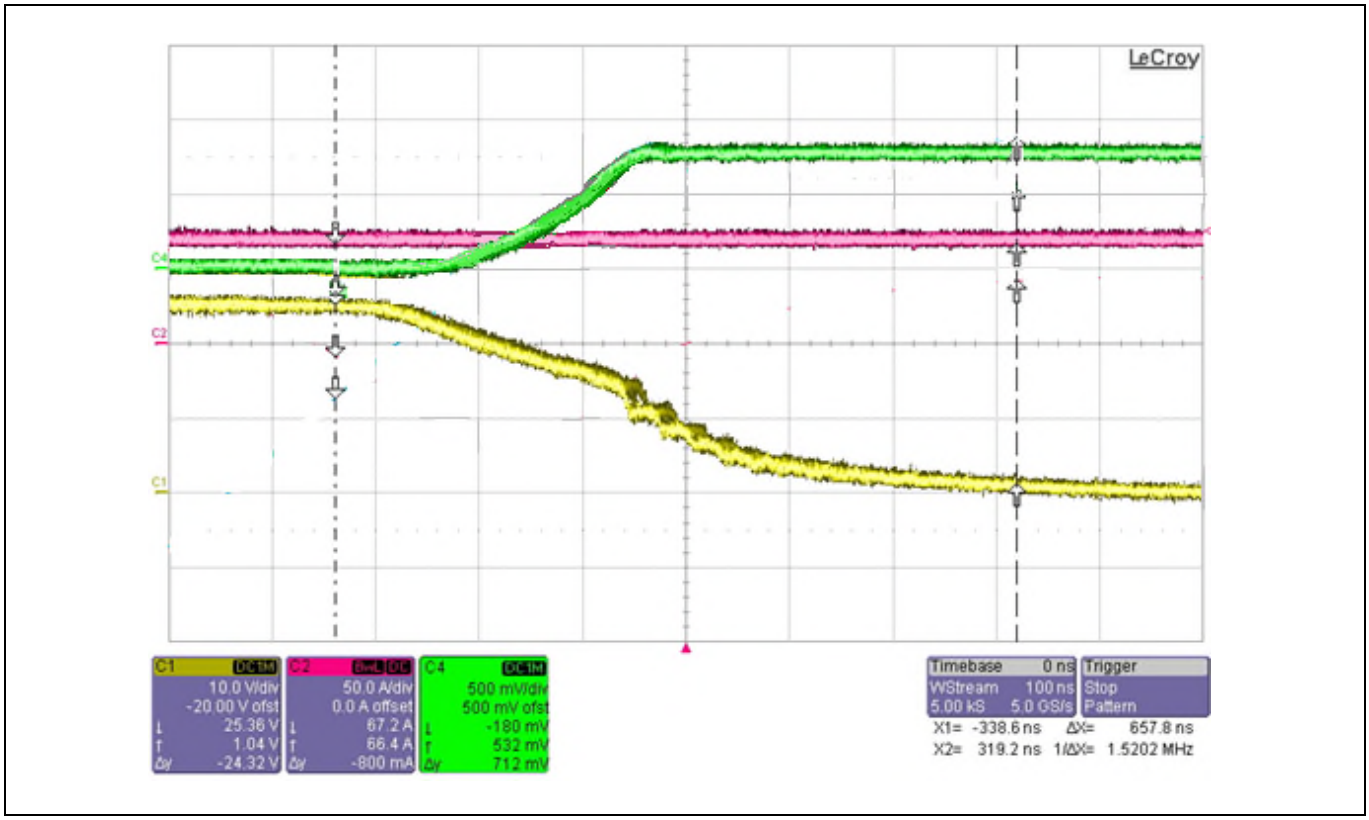

Figure 17 **Full-bridge sine-wave inverter low-side MOSFET hard switch-on**
CH1 (yellow): VDSL1, CH2 (red): Ipri, CH4 (green): IDL1

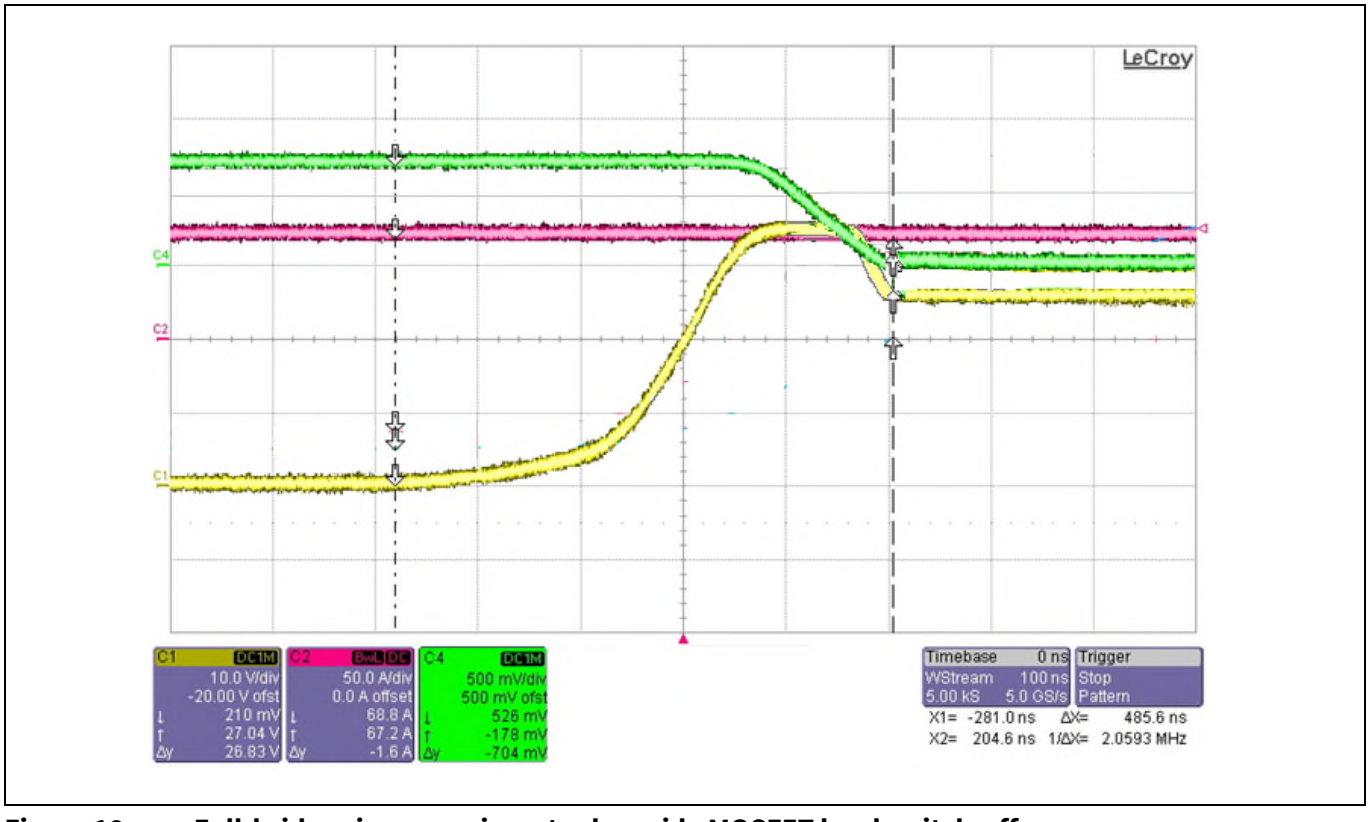

Figure 18 **Full-bridge sine-wave inverter low-side MOSFET hard switch-off**
CH1 (yellow): VDSL1, CH2 (red): Ipri, CH4 (green): IDL1

Here the drain current (green) continues to flow through the lower MOSFET during the transition until the drain voltage rises above the corresponding high-side MOSFET body diode, allowing the current to be diverted through it. The forward recovery of the body diode is responsible for the brief excursion of the drain voltage above the battery voltage, which occurs for ~150 ns. This explains why MOSFETs with BV_{DSS} rated at 40 V or above are required for a 24 V battery-based full-bridge design.

In many cases it is not feasible to use a single MOSFET in each switch position. To arrive at a practical solution the thermal properties of the package and the size of the heatsink as well as the available forced air cooling within the enclosure must all be carefully examined.

3.4 Body diode reverse recovery loss

Another significant source of losses that exists in full-bridge inverters is caused by the reverse recovery of the body diode of the upper MOSFETs when the corresponding lower MOSFET turns on. During the dead-time the inductor primary current passes through the body diode and when the low-side switches on this current is diverted through the channel of the lower MOSFET. The high-side MOSFET body diode reverse recovery causes an additional current to flow through it from the battery to ground via the lower MOSFET, creating a current spike in addition to the load current. This increases the switch-on losses in both the upper and lower devices, and it is therefore beneficial to select parts with lower reverse recovery charge (Q_{rr}) and time (t_{rr}). To minimize this the MOSFET gate-drive circuit is designed so that the device does not switch on too rapidly.

When considering MOSFETs in parallel it becomes clear that during the dead-time more current will flow through the upper MOSFET, whose body diode has the lowest forward voltage. If the parallel parts are not well matched most of the current could be flowing through one body diode. In this case most of the transient current during reverse recovery would also pass through the same device, creating high losses and stress in that device. Again it becomes clear that parallel devices should be as well matched as possible to minimize potential field failures due to the over-stressing of one MOSFET.

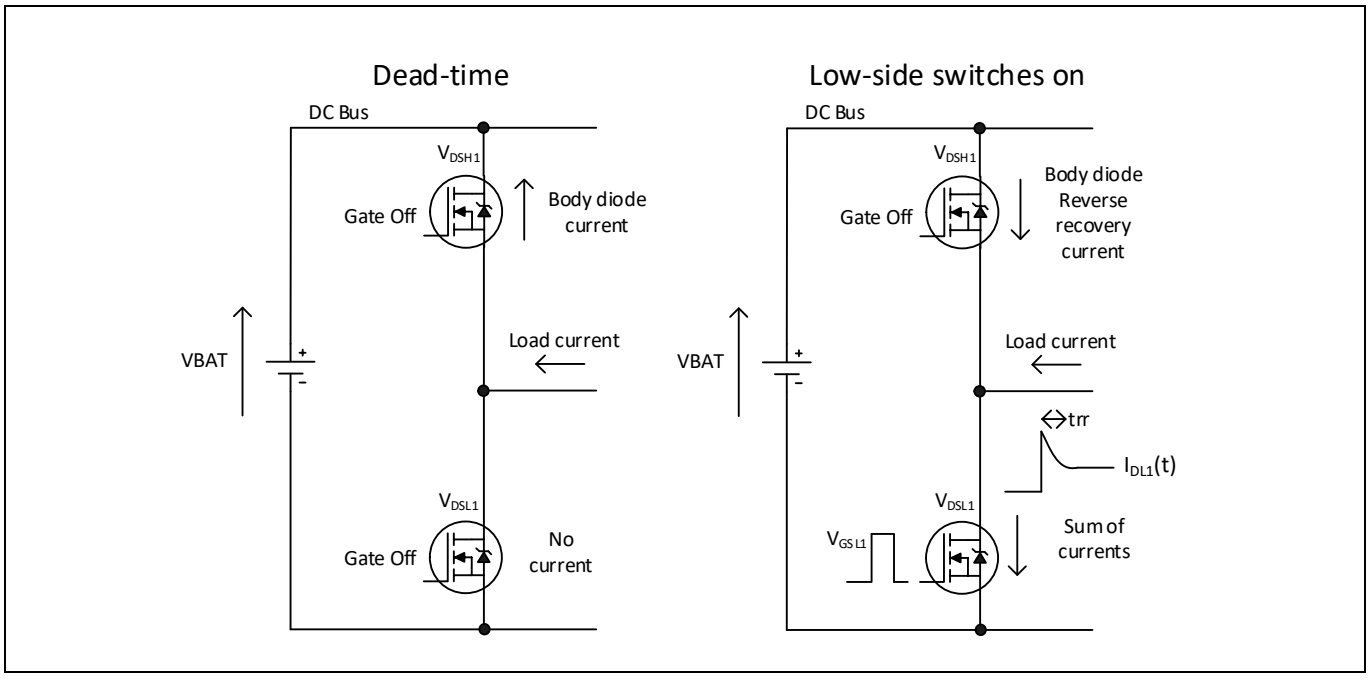

Figure 19 Body diode reverse recovery at turn-on

3.5 Conduction losses

Steady-state conductions are relatively easy to calculate from the highest load current reflected to the transformer primary and multiplied by the combined parallel $R_{DS(on)}$ of each individual bank of MOSFETs. The average drain current in each MOSFET can be estimated as follows:

$$I_{D(FET)} = \frac{P_{LOAD(MAX)} \cdot N_S}{2 \cdot V_{AC(OUT)} \cdot N_P \cdot N_{FETS}} \quad [3]$$

Where N_P and N_S are the transformer turns (only the ratio is needed) and N_{FETS} is the number of parallel MOSFETs per switch bank. Once $I_{D(FET)}$ has been determined, the conduction loss per MOSFET can be calculated from:

$$P_{C(FET)} = I_{D(FET)}^2 \cdot R_{DS(ON)} \cdot D \quad [4]$$

where D is the duty cycle.

3.6 Switching loss calculation

Switching losses can be estimated from a calculation following the general formula:

$$P_{SW(FET)} = (E_{LOSS(ON)} + E_{LOSS(OFF)}) \cdot f_{SW} \quad [5]$$

where the energy per switch-on transition and the energy per switch-off transition are each estimated then added together and multiplied by the switching frequency. The switching energies can be derived from a linear approximation from reference [2], using the following formulae:

$$E_{LOSS(ON)} = V_{BUS} \cdot \left(I_D \cdot \frac{tri+tfu}{2} + Q_{rr} \right) + \frac{Q_{rr} \cdot V_{BUS}}{4} \quad [6]$$

$$E_{LOSS(OFF)} = V_{BUS} \cdot I_D \cdot \frac{tru+tfi}{2} \quad [7]$$

assuming that the transformer inductance is high and the current ripple is small so that I_D will not change by much from switch-on to switch-off. Q_{rr} and t_{rr} can be taken from the datasheet based on device test measurements, but to utilize these equations the values of tri, tfu, tru and tfi first need to be obtained. The

worst-case current rise-time tri and fall-time tfi can be taken from the values of tr and tf quoted in the datasheet.

$$tfu = (V_{BUS} - R_{DS(on)} \cdot I_D) \cdot R_G \cdot \frac{C_{GD1}+C_{GD2}}{2 \cdot (V_{dr}-V_{plateau})} \quad [8]$$

where the two values C_{GD1} and C_{GD2} can be extrapolated from the datasheet graph as follows:

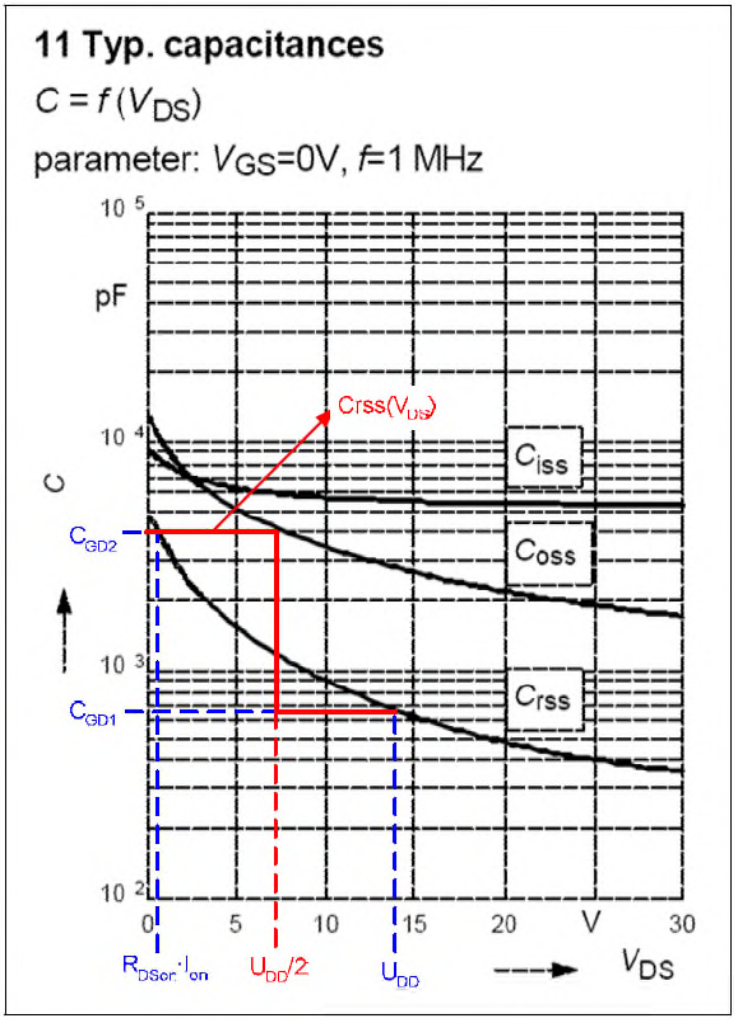

Figure 20 Two-point representation of gate-drain capacitance from a power MOSFET

$$tru = (V_{BUS} - R_{DS(on)} \cdot I_D) \cdot R_G \cdot \frac{C_{GD1}+C_{GD2}}{2 \cdot V_{plateau}} \quad [9]$$

With these values the switching losses can be calculated.

Conduction and thermal losses contribute to die temperature rise. To avoid device failure the die temperature cannot exceed specified limits. To ensure this switching transitions must within the defined Safe Operating Area (SOA).

3.7 How many parallel MOSFETs should be used?

As previously mentioned in Section 2, the paralleling of MOSFETs for power handling is non-trivial, with many factors to take into account.

3.7.1 Gate threshold, $V_{GS(th)}$

Gate threshold in hard-switching applications may not be too low, otherwise the converter will be susceptible to induced turn-off of the corresponding device in the half-bridge during switch-on. Standard gate threshold devices are best suited to UPS.

Supposing two or more MOSFETs are used in parallel to form each switching element, there is a tolerance of gate threshold voltage for the specific MOSFET such that each device has a different gate threshold. In some cases one device may have a significantly lower gate threshold than the others. Assuming the gate-drive voltage is sufficiently high, this will not cause any appreciable current sharing imbalance during the on-state; however, the device with the lower threshold will switch on before the others. In that case since the rise-time of the gate drive is finite, all of the current will flow through one device for a brief period until the other devices also switch on. This means that the SOA should be considered for a single device during switch-on unless the gate thresholds have been selected to match each other closely.

In addition, at switch-off the device with the lowest gate threshold will switch off slightly later than all of the others, again having to sustain the full current during the switch-off transition. During the on-state the current is shared between each device, facilitated by the positive temperature coefficient of $R_{DS(on)}$. This functions because the V_{DS} values of each parallel device must be equal; therefore, a lower $R_{DS(on)}$ part carries a greater share of the current, dissipating more power and heating more rapidly. This causes $R_{DS(on)}$ to rise, which then reduces the current so that more diverts through other parallel devices, preventing thermal runaway in any single MOSFET. It does however takes a finite time for the device currents to reach a state of equilibrium, therefore currents are unlikely to be evenly distributed between MOSFETs during the switching transitions. Additional source resistors could be added to provide negative feedback and futher equalize the currents, but the additional power losses make this solution undesirable.

The gate-drive circuit requires a driver with sufficient sink and source capability to support the combined gate charges of several MOSFETs in parallel. Each MOSFET will require its own gate-drive network connected to a common gate driver.

3.7.2 Avalanche voltage, BV_{DSS} or $V_{(BR)DSS}$

The avalanche breakdown voltages of each parallel MOSFET will inevitably vary. It is therefore evident that the device with the lowest BV_{DSS} will absorb all of the energy from a clamped transient voltage. For this reason the designer must consider the maximum avalanche energy rating of a single device for withstanding the transients that appear in the application. As mentioned, the push-pull topology produces larger transients with more energy to absorb when clamping, and therefore it becomes necessary to select devices BV_{DSS} rated somewhat higher than two times the highest battery voltage. In the case of a full-bridge topology the transients are smaller and contain less energy. Despite this, it is advisable to also leave a large safety margin for BV_{DSS}.

Having considered the worst-case BV_{DSS} during inverter operation, it is absolutely vital in LF transformer-based UPS designs to account for the highest line voltage that could occur during charging. Although this may not seem to be an issue under normal line voltage conditions, it becomes particularly important during a high-line surge. In countries where the power grid is known to vary widely, a nominal 230 V_{RMS} line voltage could rise by more than 50 percent. This is why it is essential to allow for this by evaluating the maximum the voltage that could appear at the primary winding during such an event. Clearly BV_{DSS} must be selected to be above this value otherwise one or more MOSFETs may avalanche in the event of a surge, in which case the amount of energy involved would rapidly destroy the device.

Another important consideration is avalanching that may occur due to abnormally high voltages produced during a short-circuit condition, which will be discussed further.

3.7.3 Parasitic inductances

It can be assumed that the package inductances will be similar in each parallel MOSFET; however, the PCB traces should be designed carefully to minimize parasitic inductance in the source connections and to keep these as equal as possible for each device. Parasitic inductance adds to ringing and associated losses.

Unequal trace inductances would further prevent the parallel MOSFETs from switching on and off at the same time.

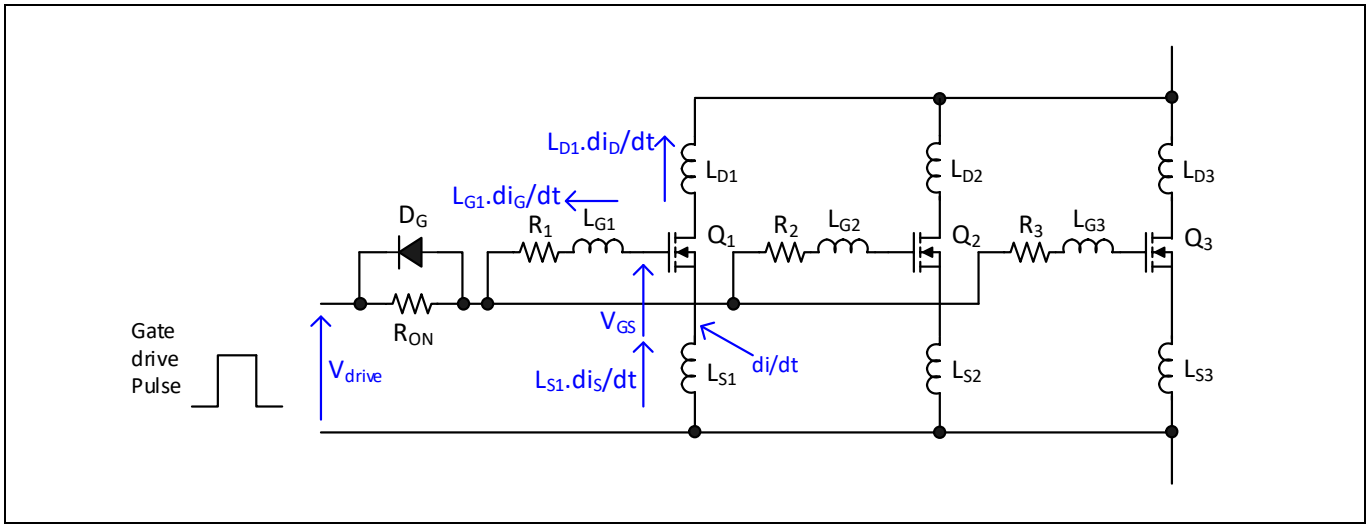

Figure 21 Parasitic inductances

Each element of parasitic inductance produces a voltage when a changing current passes through it. The larger the di/dt the larger the voltage. In the case of the gate drive the gate-to-source voltage is composed of the voltage across the source inductance subtracted from the drive voltage. Fast-changing drain current can therefore tend to drive the MOSFET off and can give rise to oscillations when combined with device capacitances, which result in switching edge ringing that introduces additional losses. The problem is made worse if the gate-drive current pulses are not sufficiently limited by series resistors, since gate inductance also produces voltage drop that is further subtracted from V_{GS} during turn-on. Damping is therefore necessary to prevent oscillations, and this is provided by the gate-drive resistors R1, R2 and R3.

3.7.4 Body diode forward voltage drop

Body diode forward voltage also varies from one MOSFET to another. The temperature coefficient is negative, therefore the body diode with the lowest forward voltage drop V_{SD} will conduct most or all of the current, and as its die temperature increases and the voltage drops further it will tend to draw more of the available current, leading to potential thermal runaway and failure.

Though this may not be a problem during inverter operation, when diode conduction occurs for only short periods during the dead time, it becomes critical during charging. Unless the paralleled MOSFETs have similar V_{SD} values all of the charge current will pass mostly through the body diode of the MOSFET with the lowest V_{SD}. In the case of a push-pull topology the peak current may be in the region of 100 A, and this may exceed the maximum body diode source current rating for a single MOSFET, which must be considered at an elevated temperature such as 100 degrees C. A maximum pulse current rating may be used to determine whether the MOSFET is being used within specifications. MOSFET datasheets typically quote such a rating where the pulse width is limited by maximum junction temperature.

3.7.5 Short-circuit output condition

Although the MOSFET parameters and the number of devices placed in parallel in each switch position of the inverter may be sufficient to allow for steady-state operation at maximum load and charging, it is also essential to consider the case when the UPS output is short-circuited. A typical UPS with a LF transformer includes a current-sense shunt connected to a protection circuit that shuts off the MOSFET gate drives in under 2 µs if an abnormally high current is detected. Though the high inductance of the transformer primary and less than perfect coupling limit the rise of the primary current under short-circuit, it still rises much higher than the maximum load current before shutdown. The MOSFETs can withstand such a current pulse for a short time only before the junction overheats and the device fails by one of the following two mechanisms:

1. Thermal failure due to excessive current exceeding SOA limits and destroying the device.
2. Avalanche failure caused when the MOSFET turns off due to excessive di/dt, which creates a large drain voltage transient requiring more than the avalanche energy rating of the MOSFET to clamp it. This is likely to cause device failure.

In the inverter stage of a HF transformer-based UPS the transformer is located in the DC to DC stage, and the inverter is connected directly to the output through a low-pass filter, which normally consists of a series ferrite inductor and parallel output capacitor. The filter inductance does not provide the same current rise-time limiting as in the LF transformer case, therefore the inverter MOSFETs in such systems are subjected to higher currents before shutting down during an output short-circuit.

Even though parallel MOSFETs normally share current due to the positive temperature coefficient of $R_{DS(on)}$, in the case of a very rapid high current event there is insufficient time for equilibrium to be reached. This means that a disproportionate share of the short-circuit current may pass through one MOSFET. Since this is the case MOSFETs must be selected that have a sufficiently high pulse current rating.

3.7.6 Start-up output condition

At inverter start-up an abnormally high current may also occur. This could be due to residual flux in the transformer and/or capacitors that require charging. In this case the high current would not be high enough to trigger the protection circuitry, but could be expected to be present for a period of tens of milliseconds. In this case the current could be expected to be distributed more evenly between parallel devices. Again, the

maximum pulse current rating of the MOSFET and the number of parallel devices should allow for this condition.

Many UPS inverters incorporate a soft-start function to reduce stresses on the components during the power-up phase; however, when the AC mains supply fails a rapid start of the inverter is necessary.

All of the above factors should be considered at the MOSFET maximum operating temperatures within the application. This will be discussed further.

3.8 Gate-drive network

In hard-switching applications it is necessary to design the gate-drive network to limit the switch-on speed to avoid excessive dv/dt and di/dt as well as to allow for body diode reverse recovery. Shoot-through current resulting from body diode reverse recovery is significantly reduced when switch-on takes place gradually over a period of typically 200 to 300 ns in this application. However, during the switch-on process the MOSFET passes through the saturation region as the drain voltage falls toward zero and finally enters the ohmic “triode” region. It is therefore important to ensure that switch-on occurs rapidly enough to maintain operation within the SOA. This is important since operation outside the SOA is likely to cause deterioration of the device and decreases its reliability. In severe cases of SOA violation a catastrophic failure can occur. To verify that the MOSFET stays within the SOA it is necessary to understand the application and the time-dependent voltage and current functions.

Preventing high dv/dt in the high-side of a MOSFET half-bridge also avoids induced turn-on of the lower MOSFET when the upper MOSFET switches on. This is caused when a high drain dv/dt coupled through the gate-to-drain capacitance creates an unwanted gate voltage pulse. It is necessary to maintain a strong gate turn-off to avoid this problem. The gate-drive network therefore needs to provide a limited turn-on speed and a rapid turn-off.

When driving several devices in parallel it is also advisable for each gate to have its own resistor rather than connect the gates together directly. This helps to prevent gate oscillations and reduce the effect of dv/dv coupling between devices.

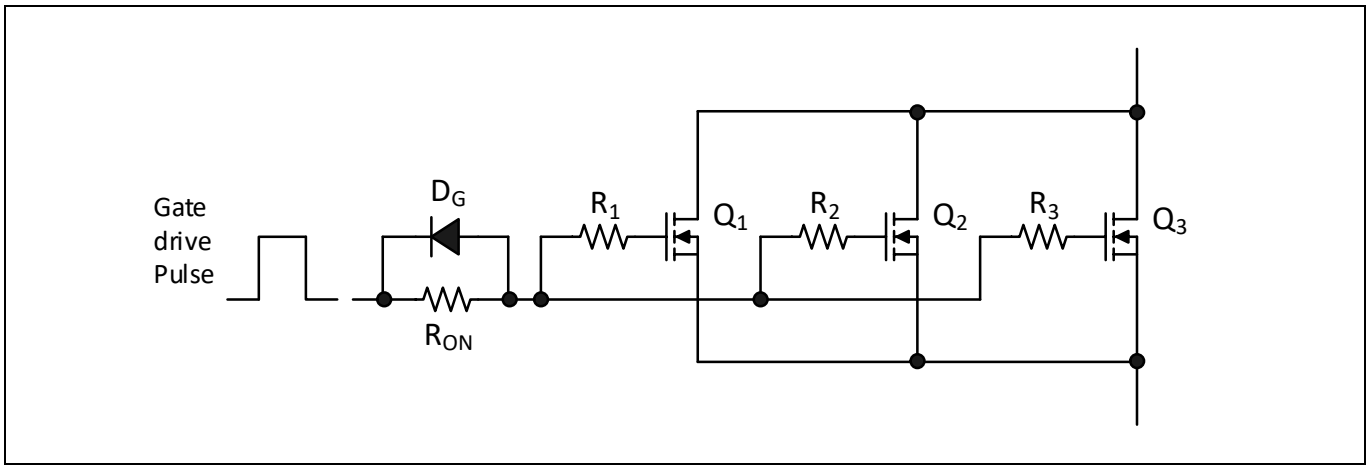

Figure 22 A typical UPS gate-drive circuit

R_{ON} is a higher ohmic value than R1, 2 and 3 to reduce the turn-on time. It is bypassed through DG during turn-off to provide a fast turn-off with strong pull-down.

4 Thermal design, MOSFET packages and heatsinks

Having considered all of the design points listed in the previous section, the next stage is to determine the necessary heatsink size and cooling for the MOSFET configuration selected. The majority of UPS systems are forced air cooled, so the temperature rise of the heatsinks depends on the speed of air flow, volume and surface area as well as the internal physical layout of the UPS. The internal placement of fans and heatsinks strongly influences how effectively the air flow removes heat. MOSFET package thermal resistance from junction to case and from case to heatsink will dictate the temperature the die reaches above the heatsink temperature.

Thermal simulations may be performed to discover what the MOSFET package temperature and die temperature are likely to be under worst-case operating conditions at maximum rated ambient temperature. Thermal performance should be evaluated with the unit in its enclosure to obtain results that accurately represent real-world conditions.

4.1 MOSFET temperature de-rating

With multiple parameters and paralleling condiderations, selecting the MOSFET for a UPS is not a simple task. A method has been provided for making an initial estimate of the power losses, which are composed of conduction and switching losses. This method uses available system and datasheet parameters to calculate these losses with enough accuracy to determine whether a certain device or combination of parallel devices is sufficient.

When the expected power dissipation per device has been calculated and it is within the maximum specification limits, then this value can be used to determine the temperature rise for a heatsink. An initial estimate of the heatsink temperature may be carried out using the thermal resistance of the heatsink to the surrounding air in degrees Centigrade per Watt under the air-flow conditions that will be present in the system. This is multiplied by the total power loss of all of the MOSFETs mounted to it to obtain the temperature rise, which is added to the maximum ambient temperature to arrive at the maximum heatsink temperature, which should not exceed 80 degrees Centigrade otherwise a larger heatsink is required. This calculation is an approximation that does not account for non-uniform heat distribution. A full thermal simulation provides a much more accurate picture and is also able to model air flow, heatsink shape and the placement of the MOSFETs with the thermal resistances between their packages and the heatsink surface. The temperature rise can be simulated as well as steady-state, and temperatures can be observed at various locations and also at the MOSFET junctions.

In a practical design the MOSFET package temperature should not exceed 80 degrees C. It is useful to make some estimates of the power dissipation for each MOSFET, which is composed of conduction losses and switching losses.

Example

A full-bridge consisting of four switches, each made up of three parallel IRFB7545 devices rated at 60 V, 95 A, 5.79 mΩ maximum.

Conduction losses are relatively easy to estimate from equation [4].

In a typical application the peak current could be 75 A with a 50 percent duty cycle. $R_{DS(on)}$ increases by a factor of approximately 1.5 at 100 degrees C. In a scenario where three parallel MOSFETs are used, the current could be assumed to be 25 A in each device. If each device has a maximum $R_{DS(on)}$ of 8.7 mΩ at an estimated die temperature of 100 degrees C, then the conduction losses would be $25^2 \times 0.0087 \times 0.5 = 2.72$ W.

Switching losses can be estimated from the method described in Section 3.6.

Rise-time tri and fall-time tfi can be taken from the values of tr and tf quoted in the datasheet:

tri = 72 ns, tfi = 43 ns

The bus voltage will be taken as 13 V and I_D is 25 A per device for the calculation, therefore:

C_{GD1} = 300 pF and C_{GD2} = 400 pF

R_G is 2.3 Ω, V_{dr} is 12 V and $V_{plateau}$ is 5 V (taken from Figure 8 of the datasheet),
trr is 37 ns and Q_{rr} is 48 nC (at T_J = 125°C).

$$tfu = (V_{BUS} - R_{DS(on)} \cdot I_D) \cdot R_G \cdot \frac{C_{GD1} + C_{GD2}}{2 \cdot (V_{dr} - V_{plateau})}$$

$$(13 - 8.7 \cdot 10^{-3} \cdot 25) \cdot 2.3 \cdot \frac{300 \cdot 10^{-12} + 400 \cdot 10^{-12}}{12 - 5} = 2.94\ ns$$

$$tru = (V_{BUS} - R_{DS(on)} \cdot I_D) \cdot R_G \cdot \frac{C_{GD1} + C_{GD2}}{2 \cdot V_{plateau}}$$

$$(13 - 8.7 \cdot 10^{-3} \cdot 25) \cdot 2.3 \cdot \frac{300 \cdot 10^{-12} + 400 \cdot 10^{-12}}{2 \cdot 5} = 4.12\ ns$$

$$E_{LOSS(ON)} = V_{BUS} \cdot \left(I_D \cdot \frac{tri+tfu}{2} + Q_{rr}\right) + \frac{Q_{rr} \cdot V_{BUS}}{4}$$

$$13 \cdot \left(25 \cdot \frac{72 \cdot 10^{-9} + 2.94 \cdot 10^{-9}}{2} + 48 \cdot 10^{-9}\right) + \frac{48 \cdot 10^{-9} \cdot 13}{4} = 12.7\ \mu J$$

$$E_{LOSS(OFF)} = V_{BUS} \cdot I_D \cdot \frac{tru+tfi}{2}$$

$$13 \cdot 25 \cdot \frac{4.12 \cdot 10^{-9} + 43 \cdot 10^{-9}}{2} = 8.0\ \mu J$$

$$P_{SW(FET)} = (E_{LOSS(ON)} + E_{LOSS(OFF)}) \cdot f_{SW}$$

$$(12.7 \cdot 10^{-6} + 8.0 \cdot 10^{-6}) \cdot 15 \cdot 10^{3} = 0.31\,\text{W}$$

Total losses per device are therefore approximately 3 W, which are 90 percent conduction losses in this case.

Since there are a total of 12 MOSFETs the combined power loss will be 36 W. Clearly a substantial heatsink with forced air cooling is required.

4.2 Thermal modeling

Thermal models for electrical power systems can be produced using the electrically analogous values of thermal resistance (Rth) expressed in degrees C per Watt and thermal capacitance (Cth) expressed in Watt seconds per degree C. These combine to give the thermal impedance (Zth). Each element in the system is mechanically connected to the adjacent element that it transfers heat to, and each of these interfaces has its own thermal resistance and capacitance. When these values are known a model of the following form can be created:

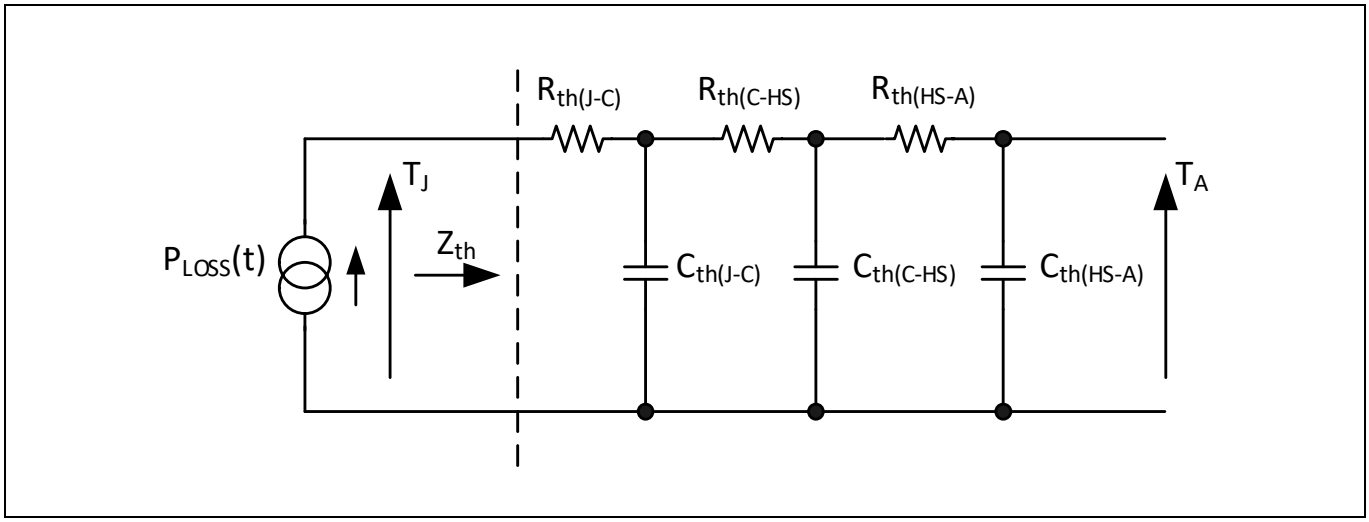

Figure 23 A typical thermal model for power elements within a UPS

It is important to keep in mind that even when an electro-mechanical system has been devised which meets thermal performance required for the application, thermal instability could also lead to MOSFET failure. A MOSFET is said to be thermally unstable if power losses produce localized heat more rapidly than it can be dissipated through the package and heatsink such that the system is not operating in thermal equilibrium. This is avoided avoided by ensuring that the thermal instability limit line in the SOA is not violated during switching.

5 Conclusion

There are many factors to be taken into account when selecting the right MOSFETs for a UPS within the lower end of the power range at levels where IGBTs do not offer benefit. The task becomes more challenging where multiple parallel MOSFETs are used to form each switch of the converter. In most cases stresses on the devices need to be considered both in *back-up mode* where the system operates as an inverter, and in *standby mode* where it operates as a battery charger. In each case the criteria for MOSFET selection are to ensure that each individual device remains within its maximum rated limits under worst-case conditions and to evaluate its power loss under steady-state conditions at maximum load and ambient temperature. In order to do this the heatsinks used in the system are designed so that they will not exceed a defined maximum temperature under worst-case operating conditions and at maximum ambient temperature. Since forced air cooling is usually used in UPS the effect of the air flow also needs to be factored into thermal evaluations.

This application note has described the architectures and topologies currently most widely used, and discussed in detail the different operating conditions and how these impact the selection of MOSFETs for long-term system reliability.

MOSFET selection can be carried out first by selecting a suitable device based on the following: BV_{DSS}, $R_{DS(on)}$, $I_{D(max)}$, $P_{(max)}$, $V_{GS(th)}$, Q_G, and Q_{rr}. Breakdown voltage and maximum current including pulsed current ratings are the most important of these, where sufficient headroom must be allowed for worst-case conditions such as high-line surges or an output short-circuit. It is essential that selection of $I_{D(max)}$ allows for high pulse currents that may occur during switching transitions where paralleled devices are not perfectly matched. $I_{D(max)}$ at a temperature of 100 degrees C should be ascertained from the MOSFET datasheet for this purpose; room temperature values quoted are not useful here. Furthermore an output short-circuit condition must be taken into account during which a current several times higher than the normal operating current will pass through the MOSFETs for up to 2 µs before the protection circuitry built into the system is able to react and force the gates low to interrupt it.

The gate threshold $V_{GS(th)}$ should not be too low to avoid possible induced turn-on in a hard-switching environment. Faster body diode reverse recovery (lower t_{rr} and Q_{rr}) will minimize inherent switching losses.

A tight tolerance is desirable so that best possible matching of parallel devices may be achieved, which will provide better current sharing during switching. Lower gate charge is an advantage, since a single gate driver is normally required to drive several devices in parallel.

Having selected a suitable candidate MOSFET, the next stage in the process is to evaluate the package and number of parallel devices to be used with the heatsinking scheme that will be used in the system. Creating a thermal model or simulation is the best method to assess the steady-state and dynamic thermal conditions within the system. This enables the designer to obtain a fair approximation of the temperatures of the heatsinks, device packages and, most importantly, the MOSFET die within the system, and to evaluate if these are acceptable or whether further modification will be necessary.

Correct design of the gate-drive circuit is of critical importance, which requires limiting the switch-on time to avoid high dv/dt and di/dt and also minimize body diode recovery while not exceeding the boundaries of the safe operating area

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